On-Chip Delay Line for Extraction of Decorrelated Phase Noise in FMCW Radar Transceiver MMICs

Alexander Melzer[1], Florian Starzer[2], Herbert Jäger[2] and Mario Huemer[1]
[1] Institute of Signal Processing, Johannes Kepler University Linz
[2] DICE Danube Integrated Circuit Engineering GmbH & Co. KG Linz

***Abstract*—Estimation of phase noise (PN) has become economically feasible for integration in many of today's semiconductors. Several contributions propose concepts that obtain a good estimate of the PN's power spectrum without even requiring a reference oscillator. Differently, in this work we aim to estimate the time domain representation of the residual PN in the intermediate frequency domain of a frequency modulated continuous wave (FMCW) radar transceiver. For that, an artificial on-chip target is utilized, which is to be incorporated into an existing monolithic microwave integrated circuit (MMIC). The estimated decorrelated phase noise is required for cancelation of short-range leakage originating from an unwanted signal reflection superimposing the overall channel response of the radar. We determine the minimum required delay such that the residual PN of the on-chip target exceeds the intrinsic noise. Further, three different realizations of the delay line in the MMIC are compared. We verify our analytical derivations with a full FMCW radar system simulation.**

I. Introduction

The phase purity of the radiated signal in frequency modulated continuous wave (FMCW) radars is a crucial design criterion. Particularly due to the high frequencies in today's radar systems, the phase noise (PN) becomes a dominant noise source affecting the detection accuracy and sensitivity. Since its origin can often not be reduced further, leakage cancelation techniques are employed in order to compensate for this introduced non-ideality.

In this work we consider an unwanted signal reflection originating from an object that is mounted right in front of the radar antennas. We denote this reflection as *short-range (SR) leakage*, which for a typical automotive application represents interspersed signals caused by the bumper. We have shown in [1] that the residual PN in the *intermediate frequency* (IF) domain raises the overall noise floor of the system. Consequently, the target detection sensitivity of the FMCW radar is deteriorated.

Although there exists a vast literature on the mitigation of leakage on chip [2,3], these concepts are not directly applicable for cancelation of the SR leakage as there are two essential differences. Firstly, the SR leakage signal power is significantly larger. This is due to the fact that the achievable isolation within the chip is well above the signal reflection factor of the SR leakage. Secondly, according to the *range correlation effect* [4], the *decorrelated phase noise* (DPN) contained in the SR leakage IF signal is notably larger than the same of the on chip leakage due to the increased propagation delay.

The *reflected power canceler* (RPC) proposed in [5] shows that almost perfect cancelation of a single radar target can be achieved if the equalizing delay is adjusted such that it matches the round trip delay time (RTDT) of an undesired signal reflection. This would also allow for cancelation of the SR leakage, however the RPC is built with discrete components, making delay lines of a wide range feasible. Within an monolithic microwave integrated circuit (MMIC) though, delay lines require a comparably large area and have a high insertion loss. The RPC is thus economically unfeasible for SR leakage cancelation within MMICs.

To overcome this issue we introduced an artificial *on-chip target* (OCT) in [6] which allows for almost perfect cancelation of the SR leakage, even if the on-chip delay is only a fraction of the RTDT of the unwanted reflection. The concept is based on the cross-correlation properties of the DPNs of the SR leakage and the OCT IF signals.

In this work we consider the implementation of such a delay line in an MMIC operating at carrier frequencies of up to 77 GHz. We derive the minimum required on-chip delay and compare transmission lines, LC delay lines and inverter chains as potential candidates for realization in hardware.

The paper is structured as follows. Section II introduces the artificial OCT used for extraction of the DPN and the SR leakage. In Section III the minimum required delay for DPN extraction is computed while in Section IV potential candidates for the delay line realization in hardware are evaluated. Finally, in Section V an FMCW radar system simulation is carried out that performs SR leakage cancelation with the proposed delay line.

II. System Model

A. Artificial On-Chip Target

The system model of the artificial OCT introduced in [6] is depicted in Fig.1. The PLL generates the chirp over a bandwidth B and duration T that is used as transmit signal defined as

$$s(t) = A\cos\left(2\pi f_0 t + \pi k t^2 + \varphi(t) + \Phi\right), \qquad (1)$$

for $t \in [0, T]$. The peak output amplitude of the PLL is A, the chirp start frequency is f_0, $k = \frac{B}{T}$ is the sweep slope, $\varphi(t)$ is the instantaneous PN, and Φ is a constant initial phase.

The OCT comprises of a delay τ_O and a gain A_O, where the latter represents the insertion loss of the delay line. Prior to entering the OCT, the transmit signal $s(t)$ is amplified by G_{DL}

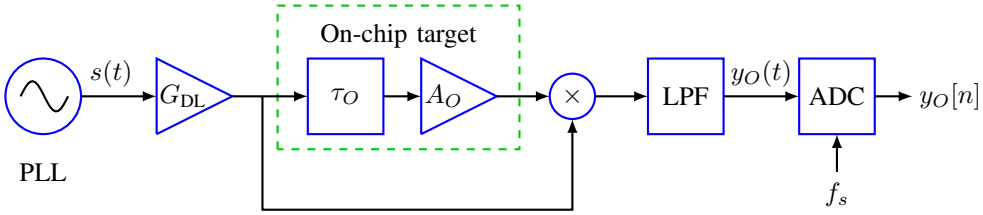

Fig. 1. On-chip target path.

to compensate for this insertion loss. Note that the structure of the OCT is similar to the well-known *delay-line discriminator* (DLD) method [7,8]. However, as will become clear later on, we use the instantaneous phase noise signal in the time domain rather than estimating the power spectral density (PSD) of the PN. Also, the OCT does not require the 90° phase shifter of the DLD method.

As depicted in Fig. 1 the OCT output signal is down-converted with the instantaneous transmit signal and lowpass filtered subsequently to remove the image. Setting the initial phase $\Phi = 0$ the lowpass filtered IF signal is

$$\begin{aligned} y_O(t) &= \left[G_{\mathrm{DL}}^2 A_O\, s(t)\, s(t-\tau_O)\right] * h_L(t) \\ &= \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \cos\left(2\pi f_{BO} t + \Phi_O + \varphi(t) - \varphi(t-\tau_O)\right), \end{aligned} \tag{2}$$

where $h_L(t)$ is the impulse response of an (ideally assumed) lowpass filter that eliminates the image originating from the mixing process, $f_{BO} = k\tau_O = \frac{B}{T}\tau_O$ is the *beat frequency* and $\Phi_O = 2\pi f_0 \tau_O - \pi k \tau_O^2$ is a constant phase term. Further, the DPN of the OCT is defined as

$$\Delta\varphi_O(t) = \varphi(t) - \varphi(t-\tau_O). \tag{3}$$

B. Extraction of the Decorrelated Phase Noise

With the cosine sum identity we can rewrite (2) as

$$\begin{aligned} y_O(t) = \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \cos(2\pi f_{BO} t + \Phi_O) \cos(\Delta\varphi_O(t)) - \\ \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \sin(2\pi f_{BO} t + \Phi_O) \sin(\Delta\varphi_O(t)). \end{aligned} \tag{4}$$

Since the phase error in (3) is sufficiently small, we can approximate (4) as

$$\begin{aligned} y_O(t) \approx \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \cos(2\pi f_{BO} t + \Phi_O) - \\ \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \sin(2\pi f_{BO} t + \Phi_O)\, \Delta\varphi_O(t), \end{aligned} \tag{5}$$

such that the DPN is extracted as

$$\Delta\varphi_O(t) \approx \frac{\frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \cos(2\pi f_{BO} t + \Phi_O) - y_O(t)}{\frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \sin(2\pi f_{BO} t + \Phi_O)}. \tag{6}$$

As depicted in Fig. 1 the OCT IF signal $y_O(t)$ is sampled with the ADC and the actual DPN extraction and SR leakage cancelation signal generation proposed in [6] are performed fully in the digital domain.

C. Short-Range Leakage

The SR leakage can be modeled in the same way as the OCT, that is with an RTDT τ_S and a gain A_S [1]. It is part of the channel, whose response is, equivalent to the OCT output signal, downconverted together with all the other target reflections. Therefore, theoretically perfect SR leakage cancelation is achieved if the reference delay τ_O matches the RTDT τ_S of the SR leakage reflection and the OCT IF signal is subtracted from the IF signal of the channel. However, since the SR target distance is considered to be in the range of a few centimeters, the required amount of delay is above one nanoseconds. This amount of delay requires a large chip area while at the same time the insertion loss would be severe, making this obvious approach infeasible.

Nevertheless we showed in [6] that there is a significant cross-correlation between the DPN of the OCT and that of the SR leakage for τ_S/τ_O ratios of up to 20. Hence a cancelation signal can be generated that achieves almost perfect suppression of the unwanted signal reflection while at the same time the amount of area required for the delay line is considerably reduced.

Unlike the channel reflections, the OCT IF signal (2) is free from channel noise and other target reflections but is perturbed by intrinsic noise only. However, from (3) it becomes clear that the DPN $\Delta\varphi_O(t)$ decreases with τ_O. This phenomenon is well known as *range correlation effect*, with the help of which the DPN power spectrum is determined as [4]

$$S_{\Delta\varphi_O \Delta\varphi_O}(f) = 2\, S_{\varphi\varphi}(f)\, (1 - \cos(2\pi f \tau_O)), \tag{7}$$

where $S_{\varphi\varphi}(f)$ is the PN power spectrum.

To conclude, a minimum delay is required such that the DPN signal power exceeds the intrinsic noise of the MMIC. The requirements for this delay line are derived in the next section.

III. Minimum Delay for DPN Estimation

According to the range correlation effect the DPN of the OCT has small amplitude for small delays τ_O. On the other hand, the OCT IF signal is perturbed by intrinsic noise of the MMIC. Thus, to obtain the DPN from the OCT with sufficient margin, the delay line must be of some minimum length. This contradicts with the initial aim to design a delay line that is as short as possible for chip area minimization. We therefore seek the minimum required OCT delay for DPN extraction in the sequel.

The total IF contribution caused by the DPN is given by the second summand in (5), that is

$$y_{O2}(t) = \frac{A^2 G_{\mathrm{DL}}^2 A_O}{2} \sin(2\pi f_{BO} t + \Phi_O)\, \Delta\varphi_O(t). \quad (8)$$

Since the DPN $\Delta\varphi_O(t)$ is a stationary random process, the power of $y_{O2}(t)$ follows to

$$\begin{aligned} P_{y_{O2}}(t) &= \mathrm{E}\{y_{O2}(t)^2\} \\ &= \underbrace{\frac{(A^2 G_{\mathrm{DL}}^2 A_O)^2}{4}}_{K} \sin^2(2\pi f_{BO} t + \Phi_O)\, \underbrace{\mathrm{E}\{\Delta\varphi_O^2(t)\}}_{P_{\Delta\varphi_O}}. \end{aligned} \quad (9)$$

With (7) the DPN power can be readily computed as

$$\begin{aligned} P_{\Delta\varphi_O} &= \mathrm{E}\{\Delta\varphi_O^2(t)\} \\ &= \int_{-B_L}^{B_L} 2\, S_{\varphi\varphi}(f)\, (1 - \cos(2\pi f \tau_O))\, df, \end{aligned} \quad (10)$$

where B_L is the bandwidth of the lowpass filter with impulse response $h_L(t)$.

Exemplarily we assume a PLL transmit power of 0 dBm, that is $A = 0.316$ V at an output resistance of $R = 50\,\Omega$. The OCT is realized with a passive delay line, which is assumed to have an insertion loss of $A_O = -20$ dB. The delay line losses are compensated using an active gain stage with $G_{\mathrm{DL}} = 14$ dB. Further, a passive mixer with a conversion gain of $G_{\mathrm{mix}} = -7$ dB is assumed.

The intrinsic noise is solely defined by the thermal noise floor at -174 dBm/Hz as both the delay line and the mixer are passive. Together with $B_L = 50$ MHz its integrated noise power becomes 0.4 nW.

With a numerical approximation of (10) and the parameters from above, $K \cdot P_{\Delta\varphi_O}$ equals the intrinsic noise for a delay of

$$\tau_{O,\min} = 60\,\mathrm{ps}. \quad (11)$$

However, in (9) the power is obtained by multiplying $K \cdot P_{\Delta\varphi_O}$ with a slow sinusoidal with beat frequency f_{BO}. Its period, that is $1/f_{BO}$, is considerably larger than the actual chirp duration. Therewith the power $P_{y_{O2}}(t)$ is highly depending on the initial phase Φ_O, which itself is a function of the delay τ_O. Since from (9) it becomes clear that the DPN is largest where the $\sin^2(\cdot)$ term has its peak value, we propose to compute the minimum delay in two steps:

1) An initial τ_O is assumed that achieves the desired SNR between the DPN power ($K \cdot P_{\Delta\varphi_O}$) and the intrinsic noise power.
2) The delay is tweaked around this initial value such that with the phase $\Phi_O = 2\pi f_0 \tau_O - \pi k \tau_O^2$ the $\sin^2(\cdot)$ is exploited around its peak value of 1.

Note that the desired SNR is achieved only at the peak value of the sinusoidal.

For our example we choose $\tau_O = 200$ ps in the first step. The resulting power $K \cdot P_{\Delta\varphi_O} = 4.8$ nW, thus an SNR to the intrinsic noise of 12 in a linear scale is achieved. In the second step we adjust the delay slightly to $\tau_O = 192$ ps, which delivers an optimum initial phase Φ_O.

To show the impact of the initial phase Φ_O, the term $K \sin^2(2\pi f_{BO} t + \Phi_O)$ as well as the total DPN contribution $y_{O2}(t)$ are depicted in Fig. 2 for our example with two different on-chip delays. In the upper plot the delay is $\tau_O = 192$ ps, while in the lower plot $\tau_O = 232$ ps. It can be observed that the resulting amplitudes for the DPN are significantly larger with $\tau_O = 192$ ps due to the resulting initial phase. For the case where $\tau_O = 232$ ps the DPN almost vanishes in the middle of the chirp.

Ultimately, with the optimized delay found in this section, the DPN extraction as defined in (6) can be employed with maximum SNR. We therefore consider a potential realization in hardware of the delay line with $\tau_O = 192$ ps.

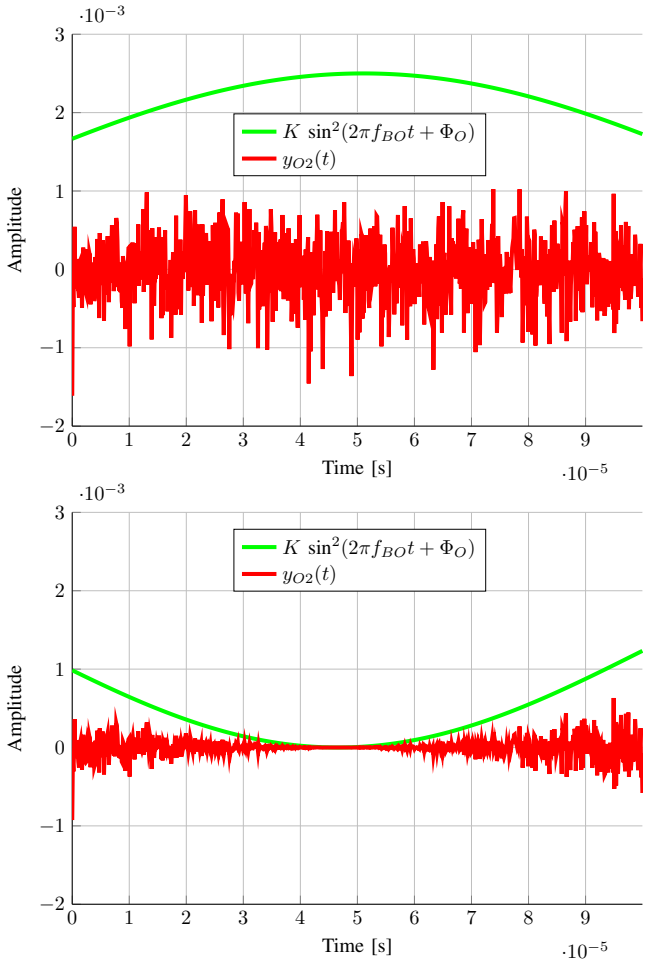

Fig. 2. OCT IF signal terms $K \sin^2(2\pi f_{BO} t + \Phi_O)$ and $y_{O2}(t)$ for $\tau_O = 192$ ps (upper plot) and $\tau_O = 232$ ps (lower plot).

IV. Delay Line Realization

In the previous section the minimum required delay for DPN extraction has been derived. We now investigate potential realizations of such a delay within MMICs for FMCW radar transceivers operating at 77 GHz. We consider transmission

lines, passive LC filters and inverter chains in SiGe:C bipolar technology with $f_{\max} = 250\,\text{GHz}$ [9]–[11].

A. Transmission lines

Transmission lines are easy to design as they simply consist of a conductor path over a ground shield. The distance between both layers and width of the lines are well defined. Its layout is typically in form of a straight line or a meander. Further, due to the passive nature only the thermal noise perturbs the signal. On the other hand, measurements show a loss in signal power of approximately $1\,\text{dB}/\text{mm}$. With a relative permittivity $\epsilon_r = 3.85$ the velocity of propagation is given as

$$c_{\text{MMIC}} = \frac{c}{\sqrt{\epsilon_r}} = 1.53 \cdot 10^8 \frac{\text{m}}{\text{s}}, \tag{12}$$

with the speed of light $c = 3 \cdot 10^8\,\text{m/s}$. Therewith, for a delay of $192\,\text{ps}$ a delay line length of approximately $2.9\,\text{cm}$ is required. Realizing this delay line using a width of $4.9\mu\text{m}$ over a $14.7\mu\text{m}$ metal shield and a spacing of $20\,\mu\text{m}$ results in an effective area of $2.9\,\text{mm} \times 180\,\mu\text{m} = 0.52\,\text{mm}^2$. The total insertion loss, or, equivalently, the noise figure is $29\,\text{dB}$.

B. Passive LC filter

An LC filter consists of a chain of inductors and capacitors, typically arranged in an LC ladder [12]. Equivalent to the transmission line it is a purely passive circuit. Acting as lowpass filter, the actual delay originates from the group delay of the filter. The critical frequency and the delay are given as [13]

$$f_c = \frac{2}{2\pi\sqrt{LC}} \tag{13}$$

and

$$\tau = \sqrt{LC}, \tag{14}$$

respectively. In order to fulfill the required frequency range of up to $77\,\text{GHz}$ we exemplarily choose $L = 0.2\,\text{nH}$ and $C = 80\,\text{fF}$. This results in $f_c = 79.58\,\text{GHz}$, $\tau = 4.0\,\text{ps}$ and an impedance of $Z_0 = \sqrt{L/C} = 50\,\Omega$. With a square spiral inductor this can be achieved with an area of $0.0013\,\text{mm}^2$ (with an outer diameter of $36\,\mu\text{m}$) [14]. Considering the size of the capacitance as comparably small, the 48 LC filters that are required to achieve $\tau_O = 192\,\text{ps}$ occupy a total area of $0.062\,\text{mm}^2$. Further, LC delay lines have a comparably low insertion loss over transmission lines. For instance, the proposed MIM-based delay line in [13] with a total delay of $276\,\text{ps}$ has a loss of merely $1.2\,\text{dB}$ for low frequencies. However, the insertion loss increases proportional to the frequency. For the problem at hand we assume it to be $20\,\text{dB}$.

C. Inverter chains

Inverter chains use the load carrier distribution in transistors to achieve a delay. For the high carrier frequencies of up to $77\,\text{GHz}$ only bipolar transistors are suitable. This results in a significantly higher current consumption as compared to a realization with CMOS technology. Different to the transmission line and the LC filter, the inverter chain is an active delay line. Consequently the noise increases with the amount of delay τ_O [15]. For the SiGe:C bipolar technology the gate delay is $3.9\,\text{ps}$ [9], therewith a total number of 50 inverters is required for the $192\,\text{ps}$ delay line. The area per inverter is assumed to be $5\,\mu\text{m}^2$, such that a total area of $0.00025\,\text{mm}^2$ is occupied.

D. Summary

An overview of the different delay line realizations is provided in Table I. Given the fact that the inverter chain has a severe impact on the current consumption, a passive delay line is considered as a more practical solution. Among the presented ones, the passive LC filter not only requires less area, but also has a considerably lower insertion loss compared to the transmission line. It is therefore a potential candidate for realization of the delay line in silicon.

V. Simulation Results

In this section a full FMCW radar system simulation is carried out. Therein the DPN from the OCT is utilized for SR leakage cancelation as proposed in [6]. The OCT path is simulated with the parameters found for the passive LC delay line in Section IV.

The PLL generates a chirp with a start frequency of $f_0 = 6\,\text{GHz}$. Typically this is $76\,\text{GHz}$ for automotive FMCW radars, however we use a lower start frequency just for computational reasons. The linear frequency ramp is carried out with a bandwidth of $B = 1\,\text{GHz}$ within a duration of $T = 100\,\mu\text{s}$.

We consider a radar channel comprising of the SR leakage in $15\,\text{cm}$ distance ($\tau_S = 1\,\text{ns}$) and a single target in $50\,\text{m}$ distance. The beat frequency of the target is therefore $3.33\,\text{MHz}$. The total noise floor in the IF signal from the channel response is known from existing measurements to be at $-140\,\text{dBm/Hz}$. As shown in Fig. 3 the PSD of the SR leakage IF signal containing the DPN exceeds this noise floor notably, thus degrading the target detection sensitivity.

To mitigate this effect we perform the SR leakage cancelation with the OCT. We therefore assume the proposed passive LC delay line with $\tau_O = 192\,\text{ps}$, $A_O = -20\,\text{dB}$. Further, we set $G_{\text{DL}} = 14\,\text{dB}$ and utilize a passive mixer with a conversion loss of $7\,\text{dB}$. With the leakage canceler proposed in [6] the DPN of the SR leakage can be estimated with that obtained from the OCT, even if the RTDT τ_S is approximately five times larger than the actual on-chip delay τ_O. As can be seen in Fig. 3, almost perfect cancelation of the unwanted signal reflection is achieved and ultimately the target in the channel is recovered well.

VI. Conclusion

In this work we investigated an on-chip delay line for estimation of the decorrelated phase noise in an FMCW radar MMIC. The minimum required delay was derived such that the DPN exceeds the intrinsic noise with sufficient SNR. Further, three different realizations of delay lines were compared with respect to their required area. The passive LC filter turned out to be a potential candidate for implementation of the delay line in silicon. Ultimately, by modeling the OCT with this delay

Delay line realization	Propagation delay	Requirement for $\tau_O = 192\,\text{ps}$	Area [mm^2]	Area [% of die size (6x6 mm)]	Insertion loss [dB]	Current consumption
Transmission line	6.7 ps / mm	2.9 cm delay line	0.52	1.4%	29	low
Passive LC filter	4.0 ps / filter	48 filters	0.062	0.17%	20	low
Inverter chain	3.9 ps / inverter	50 inverters	0.00025	0.0007%	-	high

TABLE I
COMPARISON OF POSSIBLE DELAY LINE REALIZATIONS IN MMICS WITH SIGE:C BIPOLAR TECHNOLOGY.

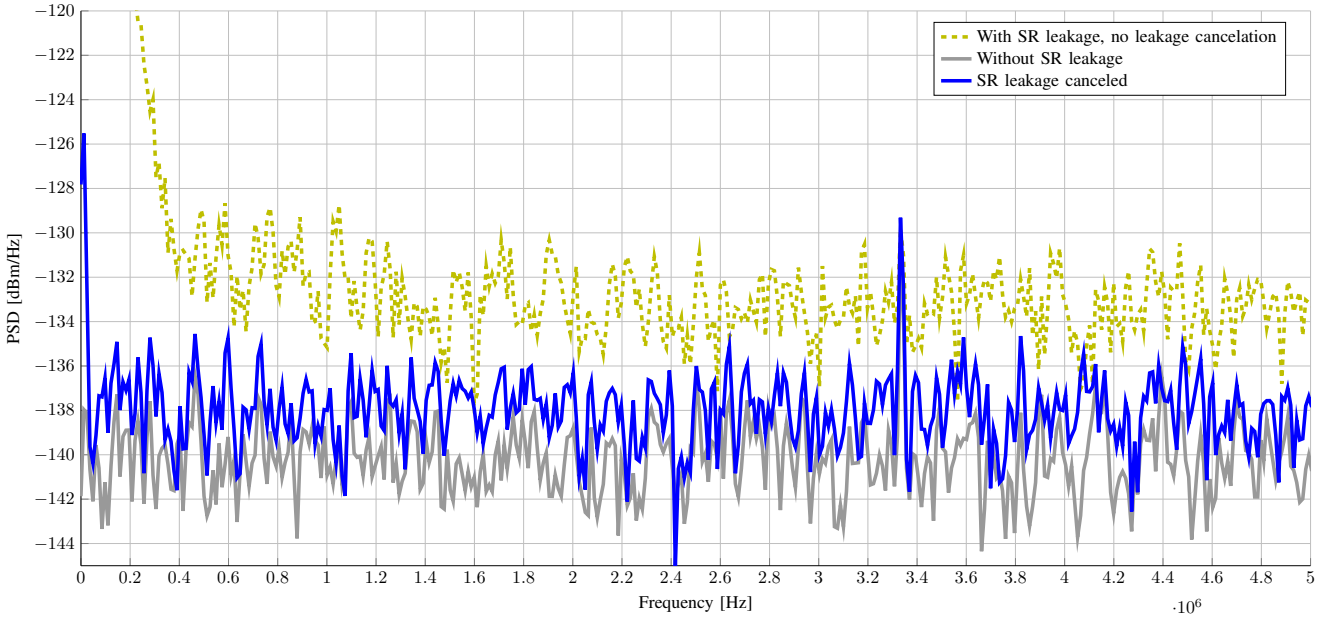

Fig. 3. Estimation of the IF PSD with/without SR leakage. It can be observed that with the SR leakage the sensitivity of the system is degraded notably. However, with the extracted DPN from the OCT, the SR leakage can be suppressed significantly and ultimately the target in the channel is recovered well.

line in an FMCW radar system simulation, almost perfect cancelation of the SR leakage is achieved.

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