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Modeling and Digital Predistortion of Capacitive Radio-Frequency Digital-to-Analog Converters

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Abstract

Wireless data transmission rates have increased significantly over the last decade and the demand continues to grow. Applications such as high-resolution video streaming require tremendous amount of data being transmitted over wireless communication channels, such as 4G or the upcoming 5G cellular networks or wireless local area networks, i.e. Wi-Fi. The demand for supporting the requirements of high data rates, robust transmissions, and power efficiency puts high constraints on the design of the transmitter of integrated communication systems.

Moreover, larger effective transmission bandwidths, 160 MHz and beyond, and higher constellation orders, exceeding 1024-QAM, will impose stringent quality requirements on the linearity and the dynamics of the transmitter. In this context, the linearity, or the linear region of a system, determines how much the wanted transmitted signal can be amplified to be transmitted over a wireless channel until it suffers from nonlinear distortions, corrupting the signal properties. However, increasing the linearity of integrated transmitter architectures typically requires to spend more power, decreasing the system's power efficiency.

In radio frequency (RF) wireless communication devices, the key component in terms of linearity and power-efficiency is the radio frequency power amplifier (RF-PA). Power-efficient implementations tend to nonlinear characteristics when increasing the signal gain, limiting the signal quality. Furthermore, increasing signal bandwidths exceeding 100 MHz, give rise to frequency dependent nonlinear effects, i.e. so-called memory effects.

A way to overcome this limitation is to use digital signal processing techniques. The input signal to the power amplifier can be modulated by a nonlinear function such that the overall system's behavior becomes linear. This technique is called digital predistortion (DPD) and is a well-known concept to increase the linear region of RF-PAs. Hence, more power-efficient RF-PA architectures can be implemented.

Another approach to increase the system's power efficiency is to utilize the advantages of integrated circuitry based on digital building blocks. Radio frequency digital-to-analog converters, so-called RF-DACs, shift the circuit complexity further to the digital domain. The RF-DAC is a key element of digital-to-RF transmitters, allowing an efficient implementation, and reducing the number of required (passive) analog circuitry. However, also the RF-DAC suffers from internal and external non-idealities, limiting the linear region of the signal amplification.

This thesis presents a close-to-circuit time-domain based modeling technique, that allows to efficiently investigate the RF-DAC's (nonlinear) characteristics. In contrast to black-box approaches, the discussed concept allows to simulate and analyze dedicated non-idealities of the RF-DAC, while still providing a significant simulation time reduction compared to circuit simulators. The modeling approach is validated by comparing it to circuit simulators, typically used black-box approaches and measurements.

Furthermore, this work introduces a circuit-inspired DPD method to cancel the

effects of supply voltage variations on the capacitive RF-DAC. The developed DPD concept re-creates the voltage distortion on the RF-DAC's supply network and modulates the input signal such that the effects on the output signal of the RF-DAC are canceled. In contrast to typically used DPD approaches, such as the (pruned) Volterra series, or memory polynomials, the complexity of the derived concept is brought down to a feasible level, allowing to be implemented on an integrated circuit. The concept is demonstrated by applying the developed DPD methodology to two different capacitive RF-DAC architectures and comparing the performance to typically used black-box models such as the (generalized) memory polynomial.

The DPD concept allows to reduce the stringent specifications of the RF-DAC's supply network while maintaining the linearity, or to improve the system's linearity by keeping the supply network performance.

Kurzfassung

Der Trend zu immer höheren Datenraten für drahtlose Kommunikationssysteme hat in den letzten Jahren erheblich zugenommen. Anwendungen wie hochauflösendes Video-Streaming erfordern die Übertragung von großen Datenmengen, wobei mobile Endgeräte auf drahtlose Mobilfunkstandards wie 4G bzw. das neue 5G oder Wireless Local Area Networks (WLAN/Wi-Fi) angewiesen sind. Die steigenden Anforderungen zum Erzielen höherer Datenraten sowie die enormen Anforderungen hinsichtlich Energieeffizienz erweisen sich als immer größere Herausforderungen für das Design integrierter Systeme.

Des Weiteren ergeben sich durch die steigenden Bandbreiten ($> 100\,\text{MHz}$) und die höhere Modulationsordnungen (1024-QAM) immer striktere Anforderungen für die Linearität von Sendern. In diesem Zusammenhang bestimmt die Linearität oder der lineare Bereich eines Senders, wie stark das zu übertragende Signal verstärkt werden kann, bis es zu nichtlinearen Verzerrungen kommt, welche die Signalqualität hinsichtlich verschiedenster Aspekte vermindern. Die Erhöhung der Linearität von integrierten Sender-Architekturen erfordert in der Regel einen erhöhten Stromverbrauch, wodurch die Effizienz des Systems verringert wird.

Bei drahtlosen Hochfrequenz (HF, engl.: RF)-Kommunikationsgeräten ist die Schlüsselkomponente in Bezug auf Linearität und Leistungseffizienz der Hochfrequenz-Leistungsverstärker (RF-PA). Leistungseffiziente Implementierungen neigen bei der Erhöhung der Signalverstärkung zu nichtlinearen Eigenschaften, wodurch die Signalqualität vermindert wird. Darüber hinaus führen erhöhte Signalbandbreiten zu zusätzlichen frequenzabhängigen nichtlinearen Effekten, so genannten *Memory Effects*.

Eine Möglichkeit die Energieeffizienz zu verbessern ist der Einsatz digitaler Signalverarbeitungstechniken. Hier wird durch eine gewollte nichtlineare Vorverzerrung des Eingangssignals des RF-PA's das Verhalten des Gesamtsystems linearisiert. Diese Technik wird als digitale Vorverzerrung (engl.: Digital Predistortion; DPD) bezeichnet, und ist ein vielfach verwendetes Konzept zur Erhöhung des linearen Verstärkungsbereichs von RF-PAs.

Ein weiterer Ansatz zur Effizienzsteigerung integrierter Kommunikationssysteme ist der Einsatz von digitalen Schaltungselementen bei der Implementierung von vormals rein analogen Schaltungen. Hochfrequenz-Digital/Analog-Wandler, so genannte RF-DACs (Radio-Frequency Digital-to-Analog Converter), verlagern die Schaltungskomplexität in die digitale Domäne und erreichen somit eine höhere Effizienz und verbesserte Skalierbarkeit. Der RF-DAC ist ein Schlüsselelement von digitalen Sender-Architekturen und ermöglicht eine effiziente Implementierung bei gleichzeitiger Reduktion der erforderlichen (passiven) analogen Schaltungselemente. Dennoch leidet auch der RF-DAC unter nichtlinearen Effekten, die den maximalen linearen Ausgangsleistungsbereich begrenzen.

In dieser Arbeit wird eine zeitbereichsbasierte Modellierungstechnik vorgestellt, welche es erlaubt, die (nichtlineare) Charakteristik von kapazitiven RF-DACs ef-

fizient zu untersuchen. Im Gegensatz zu typischen Black-Box-Ansätzen erlaubt das hier diskutierte Konzept die Simulation und Analyse von dedizierten Nicht-Idealitäten des RF-DACs. Gleichzeitig wird auch eine signifikante Verringerung der Simulationszeit im Vergleich zu Schaltungssimulatoren erreicht. Die Genauigkeit und die erforderlichen Simulationszeiten des vorgestellten Modellierungskonzeptes werden in dieser Arbeit mit Schaltungssimulatoren, konventionellen Black-Box Modellierungsansätzen sowie mit Messungen verglichen.

Des Weiteren stellt diese Arbeit eine neuartige DPD-Methode vor, mit der die Auswirkungen von Versorgungsspannungsschwankungen auf das Ausgangssignal des kapazitiven RF-DACs unterdrückt werden können. Das entwickelte DPD-Konzept bildet dabei die Spannungsschwankungen des Versorgungsnetzwerks des RF-DACs mit digitalen Modellen nach und verzerrt das digitale Eingangssignal so, dass die Auswirkungen auf das Ausgangssignal des RF-DACs unterdrückt werden. Im Gegensatz zu den üblicherweise verwendeten DPD-Modellen, wie z.B. der Volterra Reihe oder Memory Polynomials, wird die Komplexität des hergeleiteten Konzepts auf ein Maß reduziert, welches eine effiziente Implementierung auf integrierten Schaltungen ermöglicht. Die vorgestellte DPD-Methode wird an zwei verschiedenen kapazitiven RF-DAC-Architekturen getestet und mit konventionellen Modellen wie dem (General) Memory Polynomial verglichen.

Das DPD-Konzept ermöglicht es entweder die Anforderungen an das Versorgungsnetzwerk des RF-DACs bei gleichbleibender Linearität zu reduzieren oder die Linearität des RF-DACs bei gleichbleibenden Anforderungen an das Versorgungsnetzwerk zu erhöhen.

Statutory Declaration

I hereby declare that the thesis submitted is my own unaided work, that I have not used other than the sources indicated, and that all direct and indirect sources are acknowledged as references.

This printed thesis is identical with the electronic version submitted.

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Acknowledgements

Contents

1 Introduction

In recent years the demand for higher data rates in wireless communication systems has increased significantly. Latest standards such as Fifth-Generation (5G) for mobile systems and Wi-Fi 6, i.e. IEEE 802.11ax, for wireless local area networks (WLAN), increase the possible bandwidth and further also require enhanced signal quality to use higher-order modulation schemes. In addition to increasing performance requirements, systems should also operate as power-efficient as possible, decreasing operating costs of basestations and increasing battery life cycles of mobile devices. The key component in terms of performance and efficiency of a wireless transmitter is typically the radio frequency (RF) power amplifier (PA). However, power-efficient RF-PA designs tend to nonlinear characteristics. Henceforth, linearization techniques, such as digital predistortion (DPD) are required to maintain the signal quality. Another trend towards higher efficiency is to shift complexity to digital intensive circuits. A promising technology is the so-called radio frequency digital-to-analog converter (RF-DAC) [1–5], which combines the functionality of the power amplifier, the quadrature modulator (mixer), and the digital-to-analog converter (DAC) in one single component. RF-DACs use digital building blocks and thus inherently profit from technology scaling. Furthermore, these type of circuits can be implemented on the same die as the digital signal processor (DSP), pushing the RF front end closer to the digital domain. However, similar to conventional RF-PAs, DPD is required to maintain the required linearity to still guarantee an efficient design [6].

This thesis presents a novel modeling technique and a circuit inspired digital predistortion approach for capacitive RF-DAC transmitters. The modeling concept allows to decrease required simulation run times, while still keeping a close-to-circuit relation, enabling simulation and analysis of dedicated circuit-related nonidealities, including supply voltage variation and clock jitter. The second part of this work presents a detailed analysis of the effects of a varying supply voltage on the RF-DAC's output. Based on this analysis a dedicated DPD concept including memory is proposed, which modifies the input such that the supply network effects on the RF-DAC output signal are canceled.

1.1 Challenges for Wireless Transmitters

RF transmitters possess very strict requirements, where the most important characteristics are the maximum output power, the power consumption, and the linearity. Typically, the linearity is characterized by the in-band and out-of-band

performance. The in-band performance for modulation schemes applied in current cellular and Wi-Fi standards can be determined by the error vector magnitude (EVM), which is defined as the mean squared error between ideal and received samples, normalized by the average power of the ideal samples, i. e.

$$\text{EVM}_{\text{dB}} = 10 \log_{10} \frac{E\left(|s_{\text{rx}}(k,n) - s_{\text{tx}}(k,n)|^2\right)}{E\left(|s_{\text{tx}}(k,n)|^2\right)}, \tag{1.1}$$

where $s_{\text{tx}}(k,n)$ are the ideal transmitted symbols at symbol index n and subcarrier index k, and $s_{\text{rx}}(k,n)$ are the respective received symbols for the same symbol and subcarrier index, after linear equalization [7, 8]. The EVM is evaluated at the symbol level and is as such only an indicator of the in-band signal performance. For digital modulation schemes such as quadrature amplitude modulation (QAM), lower EVM allows to use higher-order alphabets, ultimately increasing the throughput of the system.

The out-of-band performance of an RF transmitter is measured based on the spectral purity, i. e. how much of the transmitted signal leakds into other channels. This so-called spectral leakage describes the undesired widening of the transmitted signal's spectrum, which may disturb communication of neighboring channels, as depicted in Figure 1.1. This phenomenon is caused by nonlinear characteristics of the transmitter circuitry, and is referred to as spectral regrowth. The bandwidth of the transmitted signal is allowed to be in a certain band. Spectral components outside the allocated bandwidth, which are generated due to nonlinearities, are superimposing the neighboring channel's communication signal. Severe performance degradation, or even complete communication losses, can be the result. The upper limits of spectral leakage are defined by communication standard authorities such as the Federal Communications Commission (FCC). One way to characterize the spectral regrowth is the adjacent channel leakage power ratio (ACLR), or adjacent channel power ratio (ACPR). The ACPR is defined as the power ratio over a defined bandwidth ΔB_1 in the ajdacent/alternate channel to the total desired transmission power

$$\text{ACPR} = \frac{\int_{f_c+f_1}^{f_c+(f_1+\Delta B_1)} S_y(f)\, df}{\int_{f_c-BW/2}^{f_c+BW/2} S_y(f)\, df}, \tag{1.2}$$

where $S_y(f)$ is the power spectral density (PSD) of the transmitted signal. The numerator in (1.2) is the adjacent channel power (ACP). Typically, the ACP, and hence the ACPR, are separated into upper and lower parts, targeting the adjacent/alternate channel on the higher or lower frequency region with respect to the carrier frequency, respectively, i. e. intervals $[f_c + f_1, f_c + f_1 + \Delta B_1]$ for upper ACPR and $[f_c - f_1 - \Delta B_1, f_c - f_1]$ for lower ACPR. Figure 1.1 depicts the PSD $S_y(f)$ of the transmitted signal, the desired channel $[f_c - BW/2, f_c + BW/2]$, and the respective adjacent channels. A so-called guard interval is usually placed between the desired signal and the neighboring channels. Furthermore, the figure also shows an example of a selected band for the ACPR (1.2). However, the ACPR

is typically evaluated for the whole adjacent channel, i.e. $[f_c + BW/2 + f_\text{guard}, f_c + BW/2 + f_\text{guard} + BW]$. In contrast to the EVM, the ACPR is a measure for out-of-band behavior. Henceforth, both measures must be used for a "complete" characterization of the transmitter's nonideal behavior.
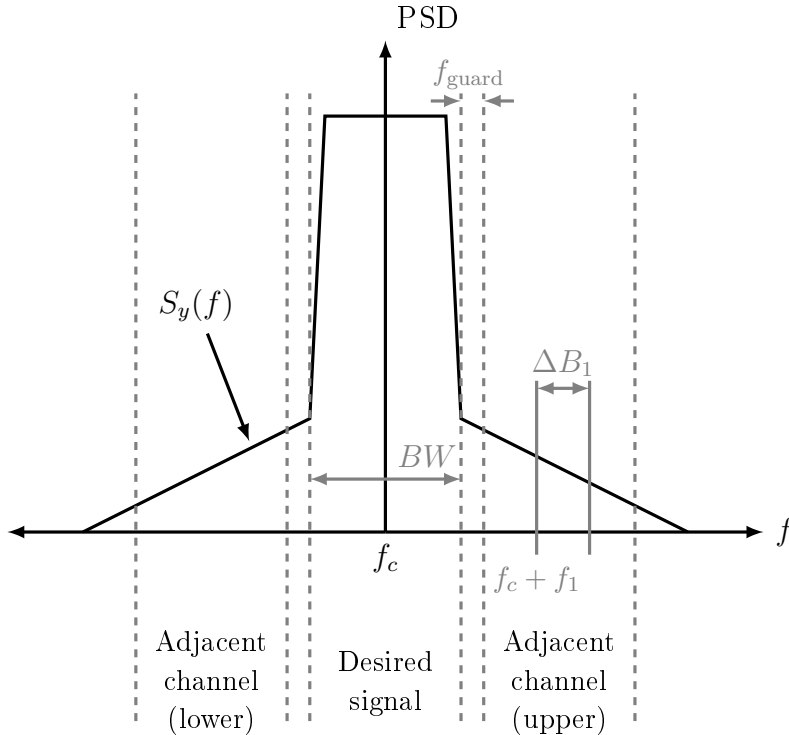
Figure 1.1: Desired, adjacent channels, and dedicated band in adjacent channel for ACPR evaluation.

In wireless transmitters, typically the RF-PA is the main contributor to the overall system's nonlinear behavior. Signal amplification always comes with the tradeoff to either sacrifice linearity or efficiency [9, 10]. Moreover, future communication systems push the limits in terms of possible bandwidth and modulation order even higher. The new Wi-Fi 6 generation, i.e. IEEE 802.11ax, already foresees baseband bandwidths of up to 160 MHz, and 1024-QAM. Such wideband signals also cause dynamic, i.e. frequency dependent, nonlinear effects in the RF-PA. These so-called memory effects are caused by thermal, biasing, supply, and matching nonidealities [11], and oppose a significant performance degradation with increasing signal bandwidth [12, 13].

One way to overcome the nonlinear problem is to operate the RF-PA in back-off mode, where the gain is still linear. However, this results in a very poor overall system efficiency. Moreover, modulation formats such as OFDM and Wideband Code Division Multiple Access (WCDMA) exhibit high peak-to-average power ratios (PAPR) of the signal envelope [14, 15]. This requires to operate the RF-PA in high back-off mode, drastically reducing its efficiency [16]. This can be partly overcome by using PAPR reduction techniques [17, 18].

Increasing demands for signal quality and power efficiency lead to the introduction of so-called linearization approaches. This concept performs a (nonlinear) equalization by modulating the input signal by a nonlinear operator such that the overall transfer characteristic including the RF-PA is ideally linear. This approach is referred to as predistortion, which allows to use RF-PAs with higher power efficiency and more nonlinear behavior, but still maintain the overall performance. From the very first analog approaches [19, 20] to modern digital predistortion concepts [7, 10, 21, 21–24], these techniques become more and more a fixed part of communication systems, especially for wireless communications, which require high linear gains and very power-efficient designs. In contrast to analog linearization techniques, DPD, especially when performed in the complex baseband, has been proven to be a very efficient method to achieve high linearity [25]. Digital linearization techniques can be seen as nonlinear equalizers, which are typically based on mathematical models of the RF-PA that reproduce the nonlinear characteristic. Typically, only input-output operators, i. e. black box or behavioral models, are used in DPD systems. These behavioral models vary from simple polynomials to very sophisticated mathematical concepts such as the Volterra series [10, 26].

Besides linearization techniques for power amplifiers, the system's efficiency can also be improved by changing its fundamental architecture. Figure 1.2 shows the simplified block diagram of a conventional direct conversion transmitter, which directly up-converts the baseband signal $\tilde{x}(t)$ to the desired RF carrier frequency f_c. The complex-valued baseband signal is composed of an in-phase and a quadrature component i. e.

$$\tilde{x}(t) = x_I(t) + i\,x_Q(t), \tag{1.3}$$

where $x_I(t)$ represents the real and $x_Q(t)$ the imaginary component. The up-converted RF signal, i. e. the passband signal, is a real-valued signal and is centered around the carrier frequency. The RF signal is in general amplitude and phase modulated, depending on the equivalent complex baseband signal (1.3), i. e.

$$x(t) = x_I(t)\,\cos\left(2\pi f_c t\right) - x_Q(t)\,\sin\left(2\pi f_c t\right), \tag{1.4}$$

where f_c is the respective (RF) carrier frequency.
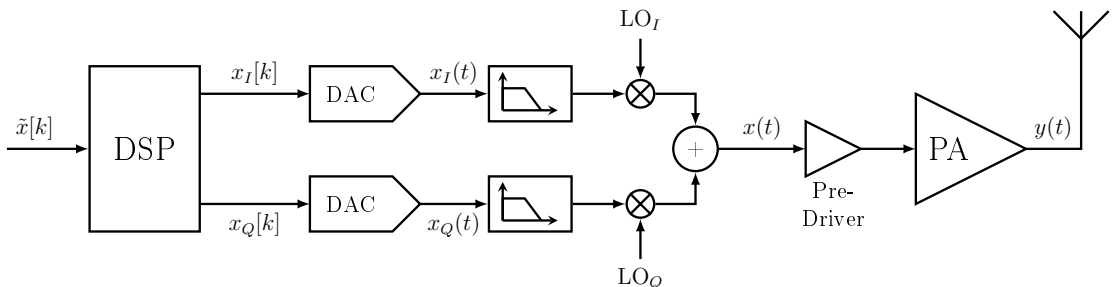
Figure 1.2: Conventional direct conversion quadrature transmitter architecture for wireless communication systems.

Such conventional transmitter architectures are mainly composed of analog circuitry, occupying most of the area and power. The DSP block, on the other hand, consists only of digital elements. DSP circuits inherently profit from technology scaling, shrinking in area and power consumption with every new generation [27]. Thus, the trend in recent years is to shift DAC and ADC closer to the antenna to perform more and more tasks in the digital parts of the system, finally targeting so-called software defined radio systems [28]. These systems directly sample at the RF frequency, ideally consisting only of the digital processing blocks and data converters. One way towards these kind of architectures is to implement the up-conversion directly inside the DAC, which is depicted in Figure 1.3. These RF-DACs have gained an increasing amount of interest in the wireless communications community [1,3,4,29,30]. Although such concepts are promising, the design becomes significantly more complicated as noise and linearity requirements are still the same as for the conventional transmitter concepts. High power RF-DACs, so-called switched-capacitor power amplifiers (SCPA) [2,31–33], also depend on a sophisticated DPD concept to maintain their efficiency [34]. Nevertheless, the increased design effort may still be profitable for the overall system as several (passive) analog components can be omitted, thus decreasing the required areas and power consumption. These approaches are especially interesting for Systems on Chip (SOC), where digital and analog components are implemented on a single die.
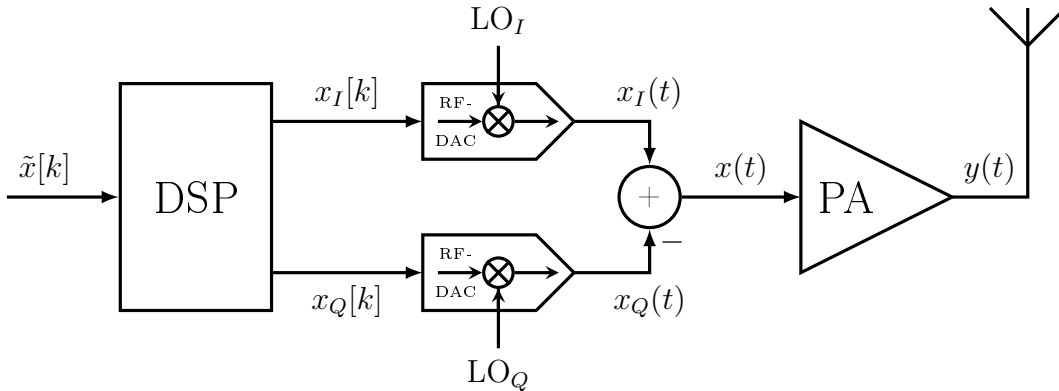
Figure 1.3: Digital transmitter architecture using a quadrature RF-DAC [3].

1.2 Undesired Nonlinear Effects in Wireless Transmitters

The nonlinear input-output characteristic of a nonlinear system such as an RF-PA is in general given by an operator $F\{\cdot\}$, which represents the complete transfer characteristic including memory effects. The output $y(t)$ is thus represented by

$$y(t) = F\{x(t)\}, \tag{1.5}$$

where the operator is applied on the input signal $x(t)$. However, in this section the RF-PA is modeled by a polynomial

$$y(t) = F\{x(t)\} = \sum_{j=1}^{J} \theta_j x^j(t), \qquad (1.6)$$

since (1.6) allows to derive the most common nonlinear effects and their respective measures. Let's assume the input to be a dual-tone signal of the form

$$\begin{aligned} x(t) &= x_1(t) + x_2(t) \\ &= A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t). \end{aligned} \qquad (1.7)$$

Signals such as (1.7) are typically used to characterize the nonlinear behavior of (RF) systems. By substituting (1.7) into (1.6) the output becomes

$$\begin{aligned} y(t) =& \theta_1 \left[A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right] \\ &+ \theta_2 \left[A_1^2 \cos^2(\omega_1 t) + A_2^2 \cos^2(\omega_2 t) + 2 A_1 A_2 \cos(\omega_1 t) \cos(\omega_2 t) \right] \\ &+ \theta_3 \left[A_1^3 \cos^3(\omega_1 t) + A_2^3 \cos^3(\omega_2 t) + 3 A_1^2 A_2 \cos^2(\omega_1 t) \cos(\omega_2 t) \right. \\ &\left. + 3 A_1 A_2^2 \cos(\omega_1 t) \cos^2(\omega_2 t) \right] + \cdots \end{aligned} \qquad (1.8)$$

It can be seen, that besides the desired output $\theta_1 \left[A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right]$ additional terms are generated, which cause undesired spectral components to appear in the spectrum of $y(t)$. These generated spectral components are called spectral regrowth. Figure 1.4 shows the output spectrum $S_y(f)$ of (1.8), considering the generated second-order and third-order distortions, which are described below.
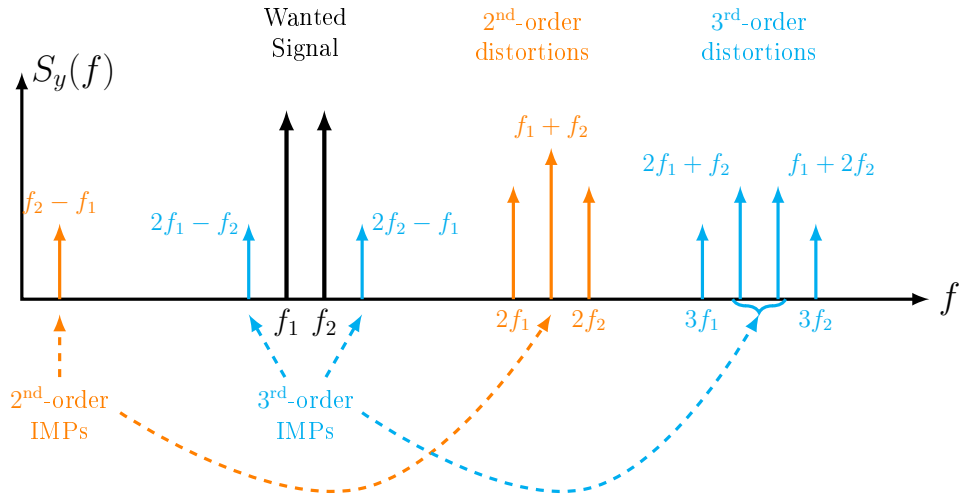
Figure 1.4: Output spectrum of a nonlinear system showing the desired signal tones at f_1 and f_2, and undesired second-order and third-order distortions.

By using the trigonometric identities

$$\cos^2 x = \frac{1}{2}\left(1 + \cos 2x\right) \tag{1.9a}$$

$$\cos^3 x = \frac{1}{4}\left(3\cos x + \cos 3x\right) \tag{1.9b}$$

$$\cos x \cdot \cos y = \frac{1}{2}\left[\cos\left(x - y\right) + \cos\left(x + y\right)\right] \tag{1.9c}$$

the second-order terms, omitting θ_2, are as follows

$$\frac{A_1^2}{2}\left[1 + \cos\left(2\omega_1 t\right)\right] \tag{1.10a}$$

$$\frac{A_2^2}{2}\left[1 + \cos\left(2\omega_2 t\right)\right] \tag{1.10b}$$

$$A_1 A_2 \left[\cos\left(\omega_1 t - \omega_2 t\right) + \cos\left(\omega_1 t + \omega_2 t\right)\right]. \tag{1.10c}$$

These kind of distortions are referred to as second-order distortions, which generate signal components at DC, twice the fundamental tone frequencies and at $\omega_1 \pm \omega_2$. Second-order distortions are typically not significant in RF-PA designs, which use differential structures and thus ideally do not produce second-order distortions. Nevertheless, for RF-PAs the third-order distortion products are more critical. Again, using the trigonometric identities, the third-order terms in (1.8) become

$$\frac{A_1^3}{4}\left[3\cos\left(\omega_1 t\right) + \cos\left(3\omega_1 t\right)\right] \tag{1.11a}$$

$$\frac{A_2^3}{4}\left[3\cos\left(\omega_2 t\right) + \cos\left(3\omega_2 t\right)\right] \tag{1.11b}$$

$$\frac{3 A_1^2 A_2}{2}\left\{\cos\left(\omega_2 t\right) + \frac{1}{2}\left[\cos\left(\left(2\omega_1 - \omega_2\right)t\right) + \cos\left(\left(2\omega_1 + \omega_2\right)t\right)\right]\right\} \tag{1.11c}$$

$$\frac{3 A_1 A_2^2}{2}\left\{\cos\left(\omega_1 t\right) + \frac{1}{2}\left[\cos\left(\left(2\omega_2 - \omega_1\right)t\right) + \cos\left(\left(\omega_1 + 2\omega_2\right)t\right)\right]\right\}. \tag{1.11d}$$

In contrast to the second-order distortions, the third-order ones directly interfere with the desired output tones at ω_1 and ω_2. Combing all terms for ω_1 gives

$$\theta_1 A_1 \left(1 + \frac{3\theta_3}{4\theta_1}A_1^2 + \frac{3\theta_3}{2\theta_1}A_2^2\right)\cos\left(\omega_1 t\right), \tag{1.12}$$

which shows that at the desired output angular frequency ω_1 the amplitude is not the desired $\theta_1 A_1$ but given by (1.12).

If $A_2 = 0$, then the output at ω_1 is solely determined by the first and second order gain θ_1 and θ_3, respectively. If the sign of θ_3 is opposite to that of θ_1 then the output tone at ω_1 is smaller than the desired linear gain θ_1. This phenomenon is called gain compression and can be expressed in decibels by [8]

$$G_c = 20\log\left|\theta_1\left(1 + \frac{3\theta_3}{4\theta_1}A_1^2\right)\right|. \tag{1.13}$$

The input signal power, where the gain is $1\,\mathrm{dB}$ lower than the desired linear gain is referred to as $1\,\mathrm{dB}$ compression point, depicted in Figure 1.5. In terms of the signal magnitude this is given by

$$-1 = 20\log\left|\theta_1\left(1 + \frac{3\theta_3}{4\theta_1}A_{1_{-1}}^2\right)\right|. \tag{1.14}$$
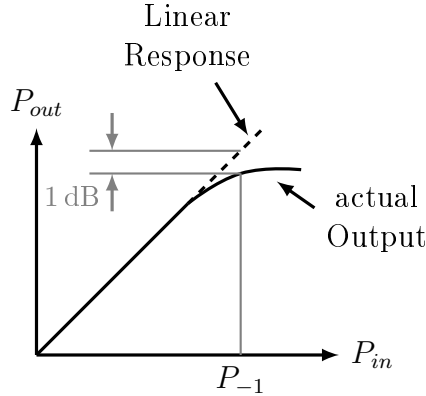
Figure 1.5: The $1\,\mathrm{dB}$ compression point is defined as the input signal power P_{-1}, where the actual output power is $1\,\mathrm{dB}$ below the desired linear gain of the system.

Expression (1.8) has spectral components at multiples of the respective tone frequencies, i. e. $m \cdot f_i$, which are referred to as m-order harmonic distortions. For example, $\frac{A_1^3}{4}\cos\left(3\omega_1 t\right)$ of (1.11) is a third-order harmonic distortion as it appears at three-times the fundamental tone frequency of $x_1(t)$. In general, a system modeled with (1.6) possesses up to J-order harmonic distortions.

Another kind of distortion, which is crucial for nonlinear system designs such as RF-PAs, is caused by the nonlinear combination of multiple tones. These so-called intermodulation products (IMP) generate spectral components in-band and out-of-band, as depicted in Figure 1.4. Beside spectral regrowth outside the desired spectrum, IMP cause intersymbol interference (ISI) and also decrease the in-band quality of the signal. Furthermore, these distortions also increase the spectral regrowth in the close out-of-band region, probably causing violations of the specified spectral limits. The power of these intermodulation products is referred to as intermodulation distortion (IMD), which is an important metric for RF-PAs. Intermodulation products are also classified by their respective frequencies. In general the m-order IMP is defined by the sum of the absolute values of the composed frequencies. For example, terms with frequencies $f_1 \pm f_2$ in (1.10) are so-called second-order IMPs, and terms having frequencies $2f_1 \pm f_2$ and $f_1 \pm 2f_2$ as in (1.11) are referred to as third-order IMPs. It is discussed in Section 2.2 that odd-order IMPs with $|m_1 + m_2| = 1$ for $m_1\,f_1 + m_2\,f_2$ are of special interest for RF-PAs.

1.3 Motivation and Scope

The scope of this thesis is to analyze individual contributors of the nonlinear behavior of capacitive RF-DACs by novel modeling techniques. Based on the results a digital predistortion concept shall be developed to improve the linearity of the RF-DAC. The modeling shall provide the opportunity to simulate and analyze the specific behavior of the RF-DAC. With the digital predistortion, the linearity of the RF-DAC shall be enhanced, also for wideband signals by using a (DPD) model with memory. Furthermore, the DPD shall also be implementation friendly, i. e. allowing the use of linear estimation algorithms and reduce the number of required coefficients.

State-of-the-art behavioral models such as the Volterra series reflect only the input-output characteristic of a nonlinear device [26, 35]. While this is often sufficient for DPD approaches, this methodology does not allow to analyze and simulate individual contributions of the overall system's nonlinearity. In early design phases of integrated circuits, it is important to understand the impact of several nonidealities such as supply voltage variation or clock jitter. On the other hand, circuit design tools such as SPICE allow accurate simulation of analog components on transistor level, but require tremendous amount of computational power and simulation time. This is even worse for digital intensive converters such as the RF-DAC, which operate in two frequency regions, i. e. the baseband input signal in the few MHz range and the RF output signal at several GHz. Due to the switching behavior of such circuits, small signal analysis provides only a limited possibility to analyze nonidealities. Hence, studying nonlinear effects requires intensive simulations in the time domain. Chapter 3 introduces an alternative, but still circuit related approach for modeling capacitive RF-DACs. The presented switched state-space approach enables accurate modeling, while significantly lowering the required simulation run time. With the presented approach, not only internal weaknesses such as capacitor mismatch, but also external nonidealities such as supply variation and clock jitter can be simulated and analyzed with the same model.

Similar as for the above mentioned modeling concepts, the black box approach may also be not the most effective solution for digital predistortion systems. In Chapter 4, this thesis introduces novel methodologies to compensate nonlinearities of the RF-DAC by the means of dedicated digital signal processing methods. While the concepts use similar techniques as conventional DPD systems, the underlying mathematical model is based on the detailed analysis of the effect of a varying supply voltage on the RF-DAC output, which is one of the most dominant contributors to the overall system's nonlinear behavior. The presented approach utilizes the RF-DAC's internal behavior, recreates the varying supply voltage and modulates the input signal such that the overall effect on the RF-DAC's output signal is canceled. It is shown, and validated by measurements, that the developed concept outperforms current state-of-the-art DPD approaches such as the (generalized) memory polynomial while even using less coefficients. With that,

an efficient pure digital based method is introduced, which allows to improve the linearity and relaxes the typically strict requirements on the supply network of the RF-DAC.

1.4 Outline of the Thesis

Chapter 1 gives an introduction to the thesis and discusses the fundamental problem of the linearity in transmitter circuits for wireless communication systems and reviews the most dominant effects of nonlinear systems. The basic concept of nonlinear modeling, using simple polynomials, is demonstrated, and the most commonly used terms, such as intermodulation distortion, are discussed.

In Chapter 2 the reader is familiarized with the fundamentals and state-of-the-art of the capacitive RF-DACs and digital predistortion. An overview of the different RF-DAC architectures, the efficiency, and a short introduction to the different origins of nonidealities is given. Moreover, the concept of digital predistortion for nonlinear transmitters, focusing on the typical use case for RF-PAs, is presented. The nowadays most widely used nonlinear behavioral models, from static to dynamic ones, are reviewed and discussed. Finally, the section gives an overview of the parameter estimation for nonlinear models in DPD systems, assuming that the output is still linear in the parameters.

Chapter 3 introduces the basic concept of switched state-space modeling. The concept is applied to the capacitive RF-DAC architecture, which is further evolved to a nonlinear switched state-space model to cover the amplitude-to-amplitude (AM-AM) and the amplitude-to-phase (AM-PM) characteristic of the capacitive RF-DAC. At last, the state-space model is extended to incorporate also external nonideal effects, including capacitor array mismatch, supply voltage variation, and clock jitter.

Chapter 4 analyzes the consequences of a varying supply voltage for the capacitive RF-DAC. This phenomenon is separated into deterministic effects, i.e. voltage ripples of a switching DC-DC converter, and stochastic effects, caused by the current feedback of the RF-DAC into a nonideal supply network. A digital compensation technique for DC-DC voltage ripples on the supply is presented. Furthermore, the chapter introduces the circuit-inspired digital predistortion concept, referred to as supply network digital predistortion (SNDPD). The SNDPD is applied to two dedicated capacitive RF-DAC designs, which is discussed in the measurement section of Chapter 4.

Chapter 5 summarizes the accomplished findings and concludes this thesis.

1.5 Contributions

Throughout the work on this thesis, the following scientific contributions have been presented and published. A number of concepts, figures, and results presented in this thesis previously appeared in these publications.

Patent Applications

- **S. Trampitsch** and D. Gruber, "Compensation of non-linearity at digital to analog converters," Feb. 20, 2018, U.S. Patent 9,900,016

Peer-Reviewed Journal Papers

- **S. Trampitsch**, J. Markovic, P. Obmann, J. Fritzin, J. Zaleski, C. Mayer, M. Fulde, H. Pretl, A. Springer, and M. Huemer, "A Nonlinear Switched State-Space Model for Capacitive RF DACs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1342-1353, Jun. 2017.

Peer-Reviewed and Presented Conference Papers

- **S. Trampitsch**, G. Knoblinger, and M. Huemer, "Switched State-Space Model for a Switched-Capacitor Power Amplifer," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 1-4.

- **S. Trampitsch**, D. Gruber, M. Lunglmayr, E. Thaller, and M. Huemer, "Digital compensation of DC-DC converter voltage ripple for Switched-Capacitor Power Amplifiers," in *Proc. IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2016, pp. 1-4.

- **S. Trampitsch**, M. Kalcher, D. Gruber, M. Lunglmayr, and M. Huemer, "Modeling non-idealities of capacitive rf-dacs with a switched state-space model," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1-5.

- P. Valet, D. Giotta, **S. Trampitsch** and A. Tonello, "Switched State-Space Model for High Speed Current-Steering Digital-to-Analog Converter," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1-5.

Additional Scientific Talks

- **S. Trampitsch**, "A Nonlinear Switched State-Space Model for Capacitive RF DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

Journal Papers under Review

- **S. Trampitsch**, M. Kalcher, H. Enzinger, D. Gruber, M. Lunglmayr, M. Huemer, "A Circuit-Inspired Digital Predistortion of Supply Network Effects for Capacitive RF-DACs," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

2 State-of-the-Art and Fundamentals

2.1 The Capacitive RF-DAC

In contrast to conventional transmitter architectures for wireless systems, the introduction of so-called radio frequency digital-to-analog converters (RF-DACs) shifts the circuit complexity further to the digital domain. The concept of the RF-DAC was introduced by Luschas et al. in [1], which combines the functionality of a DAC and a mixer in a single circuit. The RF-DAC is a key element of digital-to-RF transmitters [36], which allow an efficient implementation on a monolithic die, decreasing the number of (external) analog components, and leveraging the benefits of scaled CMOS technology with increased usage of fast and programmable digital blocks. The first implementations are based on a current steering design [29], where the respective cells are switched at the carrier frequency, directly performing the up-conversion. Another architecture of RF-DACs was introduced by Yoo et al. [30,32,37], which is based on switched capacitor circuits, showing many advantages compared to the current steering approach. The so-called switched-capacitor power amplifier (SCPA), which is a different naming for the capacitive RF-DAC, uses individual switching capacitor cells, which form a capacitive voltage divider. The (division) ratio is set by the digital input signal, determining the output voltage. The switching concept performs the direct up-conversion to the respective RF carrier frequency, similar to the current steering RF-DAC. Furthermore, the capacitive RF-DAC includes an impedance output matching network, forming a resonant circuit at the carrier frequency. This serves also as an RF bandpass filter. Additionally, the design provides a certain gain, allowing for omission of pre-amplifiers or in certain applications of the antenna RF-PA [4–6].

This section gives an overview of the capacitive RF-DAC. First, the basic concept of its operation is described. Furthermore, system-relevant parameters, such as output power and power efficiency, are discussed. The remaining subsections present different capacitive RF-DAC architectures and explain the signed operation, which is crucial for increasing the efficiency of the RF-DAC. Finally, the origins of the most dominant nonlinear effects are briefly reviewed. Details on dedicated nonlinear effects are then discussed in chapters 3 and 4, respectively.

2.1.1 Concept of the Capacitive RF-DAC

Switched-capacitor (SC) circuits have been used for a long time in versatile manners such as data converters [38], in mixed-signal data processing [39], and recently as SCPAs for wireless applications [30, 32, 33, 40]. This circuit topology became particularly attractive for implementation in modern communication systems since accurately specified capacitors are economical to design and fabricate in integrated circuits (ICs). An essential benefit of the RF-DAC concept is the superior AM-AM and AM-PM linearity [4,30]. This is an important requirement of circuits designed for spectral efficient communication standards.

The capacitive RF-DAC comprises N cells, each consisting of a capacitor C_i, with $1 \leq i \leq N$, a driving inverter, and a NAND-gate, as shown in Figure 2.1. Essentially, it forms a capacitive voltage divider, switched with the LO at the carrier frequency f_{LO}. The amplitude information $(d_1, ..., d_N)$ is fed to the NAND-gates from the digital front-end (DFE), determining the number n of active switching cells, i. e.

$$n = \sum_{i=1}^{N} d_i, \tag{2.1}$$

where the mapping of the baseband input signal $\tilde{x}[k]$ to the actual number of active switching cells depends on the RF-DAC architecture and is described in Section 2.1.3. This way, multiplication and up-conversion of the digital amplitude with the LO are achieved. Inactive cells are not switched and remain connected to ground potential. Typical capacitive RF-DAC architectures for high-end mobile communication systems consist of thousands of unitary and a few binary-weighted cells. For example, a 15-bit DAC can be realized with an array of 2^{10} unitary weighted and 5 binary-weighted capacitor cells [4].
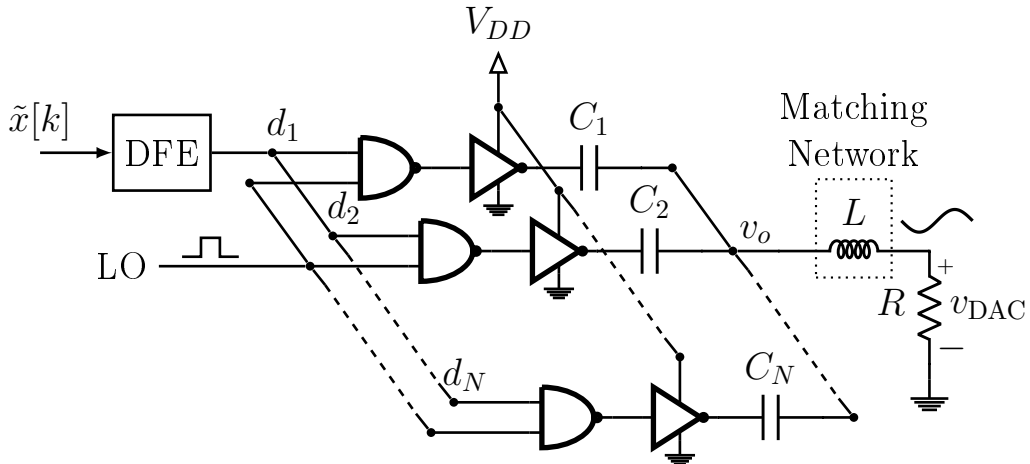
Figure 2.1: Principle circuit diagram of a capacitive RF-DAC.

For ideal operation, an equivalent circuit according to Figure 2.2 can be derived. In this circuit arrangement, a number n out of N capacitors toggle between ground

and supply voltage V_{DD}, (dis)charging with a periodicity of the (square wave) LO signal. The remaining $(N - n)$ capacitors remain connected to ground.
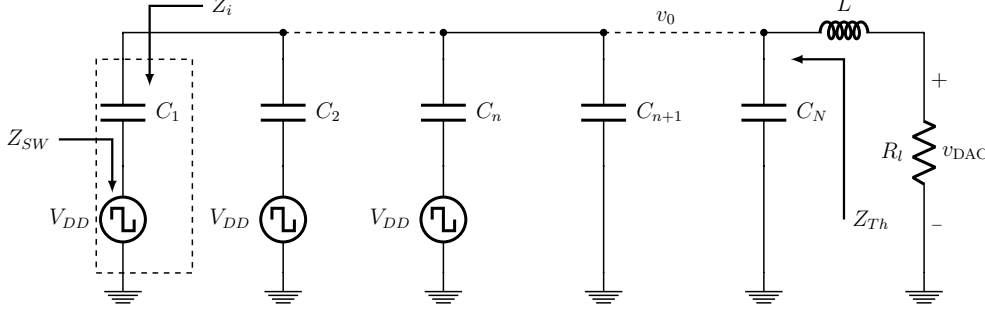
Figure 2.2: Array of N capacitors C_u. The bottom-plates of n capacitors toggle between supply V_{DD} and ground, while $(N - n)$ capacitors remain connected to ground.

An ideal capacitive RF-DAC cell is indicated by the dashed frame in Figure 2.2, with ideal output impedance

$$Z_i = \frac{1}{j\omega C_i}. \tag{2.2}$$

The switch resistance Z_{sw} is assumed to be zero. The total output impedance (Thevenin equivalent) of the ideal RF-DAC array, seen from the output matching network, is

$$Z_{Th} = \frac{1}{N} \cdot \frac{1}{j\omega C_i} = \frac{Z_i}{N} = \frac{1}{j\omega C_{\mathrm{tot}}}, \tag{2.3}$$

where the total array capacitance, $C_{\mathrm{tot}} = \sum_{i=1}^{N} C_i$, is independent of the number of switching cells n.

Without loss of generality, all capacitor cells are assumed to be unitary, i.e. $C_1 = C_2 = \ldots = C_N = C_u$. Henceforth, the total array capacitance is

$$C_{\mathrm{tot}} = \sum_{i=1}^{N} C_i = N \cdot C_u. \tag{2.4}$$

The output of an unloaded capacitive RF-DAC cell-array, i.e. without matching network, is equivalent to the voltage drop v_0 over the $(N - n)$ inactive cells as depicted in Figure 2.2. Decomposing v_0 into its Fourier series yields [41]

$$v_0(t) = V_{DD} \frac{n(t)}{N} \left(\frac{1}{2} + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left((2k-1)\omega_{\mathrm{LO}}t\right)}{2k-1} \right), \tag{2.5}$$

where $f_{\mathrm{LO}} = \omega_{\mathrm{LO}}/2\pi$ is the frequency of the fundamental tone of the LO signal. To restore a sinusoidal waveform, an (ideal) inductive element $L = \left(\omega_{\mathrm{LO}}^2 \cdot C\right)^{-1}$ is used, which resonates with the capacitive array C_{tot} at the LO's fundamental tone frequency f_{LO}. Thus, the circuit operates as a single-ended series bandpass filter with an output voltage swing

$$v_{DAC}(t) = \frac{2}{\pi} V_{DD} \frac{n(t)}{N} \sin\left(\omega_{\mathrm{LO}}t\right). \tag{2.6}$$

at the LO's fundamental tone frequency f_{LO}, assuming an ideal bandpass filter formed by capacitor array and the output matching network (OMN).

Consequently, the amplitude of the first harmonic of an unloaded capacitive RF-DAC is given by

$$V_{\text{DAC}} = \left(\frac{n}{N}\right) \frac{2}{\pi} V_{DD}. \tag{2.7}$$

Correspondingly, the output voltage amplitude can also be given by the capacitor ratio

$$V_{\text{DAC}} = \left(\frac{\sum_{i=1}^{n} C_i}{C_{\text{tot}}}\right) \frac{2}{\pi} V_{DD}, \tag{2.8}$$

or dependent on the (normalized) digital input code x_{on}

$$V_{\text{DAC}} = (x_{\text{on}}) \frac{2}{\pi} V_{DD}, \tag{2.9}$$

where

$$x_{\text{on}} = \frac{n}{N}. \tag{2.10}$$

In this thesis, (2.7)-(2.9) are used interchangeably, depending on the discussion of the respective topic. However, all equations above represent the very same relation of the output voltage amplitude to the digital input code.

The capacitive RF-DAC structure from Figure 2.1 represents a single-ended structure. This structure allows for an efficient implementation as it is only composed of one array of N capacitor cells. However, the single-ended structure imposes severe drawbacks such as bad spectral performance, high LO leakage, and highly nonlinear supply current profile [3]. Due to this, nowadays capacitive RF-DACs are built in a pseudo-differential structure, as shown in Figure 2.3. For this, a second capacitor array is required, connected to a 180° degree phase-shifted LO. Hence, this structure doubles the implementation cost. Moreover, digital decoding and clock distribution become more complicated as positive and negative capacitor arrays must switch simultaneously.

The non-switched plates of the cell capacitors of each array are connected to a transformer-based matching network, which provides a limited bandpass filtering, performs impedance matching, and additionally converts the differential voltage swing of the capacitor array to a single-ended output voltage for the load (antenna, PA). Despite the higher complexity, the performance of the pseudo-differential structure is superior in terms of noise and linearity compared to the single-ended option. Moreover, as is shown in Chapter 4, the differential architecture significantly reduces the code dependent supply voltage variation.

2.1.2 Output Power and Efficiency

The capacitive RF-DAC behaves similar to a class-D PA, allowing for high efficiency operation [32]. The ideal power-added efficiency (PAE) can be derived
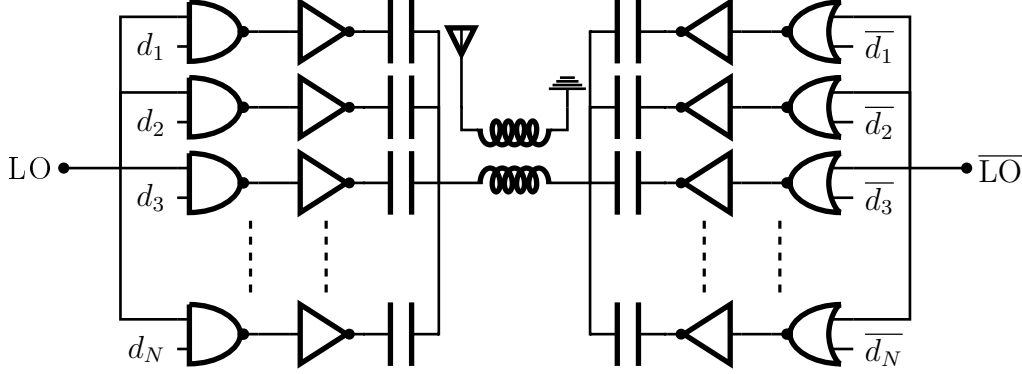
Figure 2.3: Principle circuit diagram of a pseudo-differential capacitive RF-DAC.

from a simplified Thevenin equivalent circuit, as depicted in Figure 2.4, and is given by [30]

$$\text{PAE}_{\text{ideal}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{SC}}}, \tag{2.11}$$

where P_{out} is the given output power over an ideal load resistor R_l. The output power is derived from the output voltage amplitude in (2.7) and is given by

$$P_{\text{out}} = \frac{2}{\pi^2} \left(\frac{n}{N}\right)^2 \frac{V_{DD}^2}{R_l}. \tag{2.12}$$

P_{SC} is the dynamic power required to charge and discharge the capacitor array, i. e.

$$P_{\text{SC}} = C_{\text{in}} \, V_{DD}^2 \, f_{\text{LO}}, \tag{2.13}$$

where C_{in} represents the equivalent input capacitance (no matching network) seen from the input of the capacitive RF-DAC, assuming ideal switches, i. e.

$$\begin{aligned}
C_{\text{in}} &= \frac{C_{\text{on}} \cdot C_{\text{off}}}{C_{\text{on}} + C_{\text{off}}} \\
&= \frac{n \, C_u \cdot (N - n) \, C_u}{n \, C_u + (N - n) \, C_u} \\
&= \frac{n(N - n)}{N} C_u
\end{aligned} \tag{2.14}$$

Thus, the input capacitance is at its minimum, ideally 0, if the input code is either $x_{\text{on}} = 0$ or $x_{\text{on}} = 1$. Hence the the PAE from (2.11) can ideally become 1. Nevertheless, the PAE over the whole implementation range is strongly dependent on the total capacitor array size, and the implemented matching network (inductor). Yoo et al. [30] showed that the PAE depends on the resulting quality factor (Q-factor) of the equivalent RLC resonant circuit. The resulting Q-factor is given by

$$Q_{\text{loaded}} = \frac{2\pi \, f_{\text{LO}} \, L}{R_l} = \frac{1}{2\pi \, f_{\text{LO}} \, C_{\text{tot}} \, L}. \tag{2.15}$$

Following, the resulting PAE can be derived to

$$\text{PAE}_{\text{ideal}} = \frac{4n^2}{4n^2 + \frac{\pi\,n(N-n)}{Q_{\text{loaded}}}}. \tag{2.16}$$

Including the parasitic resistance r_{on} of the driving inverters, Passamani et al. [42] extended the linear model for the efficiency of the capacitive RF-DAC to

$$\eta = \frac{P_R}{P_R + P_{\text{SW}} + P_{r_{\text{on}}}} \tag{2.17a}$$

$$= \frac{\alpha}{\beta\,(1+\alpha)^2 + (1+\alpha)}, \tag{2.17b}$$

where α represents the ratio of the load resistance to the parasitic switch (NMOS/P-MOS) resistance

$$\alpha = \frac{R_l}{r_{\text{on}}}, \tag{2.18}$$

and β is the respective technology parameter

$$\beta = \frac{2\,r_{\text{on}}\,P_{\text{SW}}}{\frac{2}{\pi}\,V_{DD}}, \tag{2.19}$$

respectively.
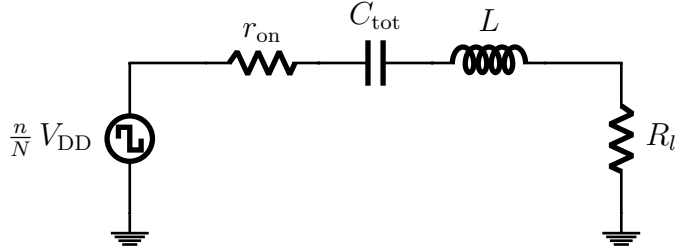
Figure 2.4: Simplified Thevenin equivalent circuit of the single-ended capacitive RF-DAC.

2.1.3 Capacitive RF-DAC Architectures

The capacitive RF-DAC can be implemented as polar or quadrature transmitter, as sketched in Figure 2.5. In the polar architecture, the DFE must provide the magnitude and the phase of the complex baseband signal. The CORDIC is a well-known digital architecture, converting quadrature data into polar representation. The respective magnitude information is processed by the decoder logic of the RF-DAC, determining the active switching cells. The output voltage magnitude is as in (2.9) depending on the input signal's magnitude, i.e. $x_{\text{on}} = |x_I + j\,x_Q|$. The phase, $\phi = \tan^{-1}\left(\frac{x_Q}{x_I}\right)$, is modulated on the phase of the LO, which is typically performed by a digital phase-locked-loop (DPLL) circuit [43]. Due to stringent

requirements of the out-of-band noise emissions for current and future cellular applications, i.e. 4G and 5G, the DPLL's integrated jitter must be below the 100 fs range [3]. Furthermore, the amplitude and phase signals possess at least three to 10 times the bandwidth of their quadrature counterpart [44], increasing the complexity of the decoding logic and the phase modulator of the LO signal. Due to the split of the phase and the magnitude information, the two data paths must be designed such that the magnitude data samples and the modulated LO are aligned at the RF-DAC. Misalignment leads to significant performance degradation, increasing the noise floor and nonlinear behavior.

For classical quadrature architectures, the cell array of the capacitive RF-DAC is split into two halfs. One half is used for in-phase and the other half for quadrature data, respectively. As for typical quadrature based transmitters, the quadrature data is mixed by a 90° phase-shifted LO, as depicted in Figure 2.5a. The in-phase and quadrature data streams are directly provided by the DFE. No additional signal processing is required, simplifying the decoder and synchronization logic. Furthermore, the PLL must only generate two fixed clock signals with a 90° phase shift. Alternatively, the respective LO clock signals can also be generated using local quadrature phase generator circuits [45, 46]. The drawback of the classical quadrature architecture is the reduced output power, and thus reduced efficiency. Assuming a capacitor array with the same size as for a polar architecture, the output voltage magnitude is

$$V_{\text{DAC,IQ}} = \frac{1}{\sqrt{2}} \left(\frac{n_I + n_Q}{N} \right) \frac{2}{\pi} V_{DD}, \tag{2.20}$$

where n_I and n_Q are the number of active cells for in-phase and quadrature cells, respectively. $\frac{1}{\sqrt{2}}$ is due to the 90° phase shift. Hence, if all cells of the quadrature capacitive RF-DAC are active, i.e. $n_I = n_Q = \frac{N}{2}$, then the maximum output amplitude is

$$V_{\text{DAC,IQ}} = \frac{1}{\sqrt{2}} \frac{2}{\pi} V_{DD}, \tag{2.21}$$

which corresponds to 3 dB less than the maximum power achieved with a polar architecture.

Another possibility is to use the so-called cell sharing technique for quadrature capacitive RF-DACs [5,6,47]. The individual cells are no longer fixed for I or Q data but can be dynamically exchanged to either the in-phase or the quadrature data stream and the respective LO signals. This method, still following (2.20), allows to achieve a maximum output amplitude equivalent to the polar architecture in (2.7) if $n_I = N$ and $n_Q = 0$, or vice versa. However, this increases the complexity of the decoder and clock distribution inside the capacitive RF-DAC, as each cell (if all are shared cells) must be connected to the in-phase and the quadrature data and LO signals through additional logic gates, respectively.

Quadrature RF-DACs, classical or cell sharing approach, are based on a weighted sum of 90° (orthogonal) phase-shifted vectors. However, the desired output vector,

in the complex plane, can also be achieved by summing non-orthogonal vectors, i. e. by using LO phases which are not 90° phase shifted. Furthermore, also the number of phases is not limited. This kind of capacitive RF-DAC is referred to as multiphase SCPA (MP-SCPA) [48]. The output voltage ratio for an MP-SCPA is given by

$$V_{\text{DAC,MP}} = \frac{\sin\left[(M-2)\frac{\pi}{M}\right]}{\left|\sin\left(\frac{2\pi}{M} - \phi\right)\right| + |\sin|\phi||}, \tag{2.22}$$

where M is the number of phases and ϕ is the wanted output phase. The maximum power loss, compared to a polar architecture, is $-0.69\,\text{dB}$ for an eight-phase or $-0.17\,\text{dB}$ for a 16-phase MP-SCPA system, respectively. However, the required DSP, and hence the implementation effort, increase significantly with the number of phases. The generation of the different LO phases tightens the already high requirements of the clock generation and the respective timing and clock distribution paths.
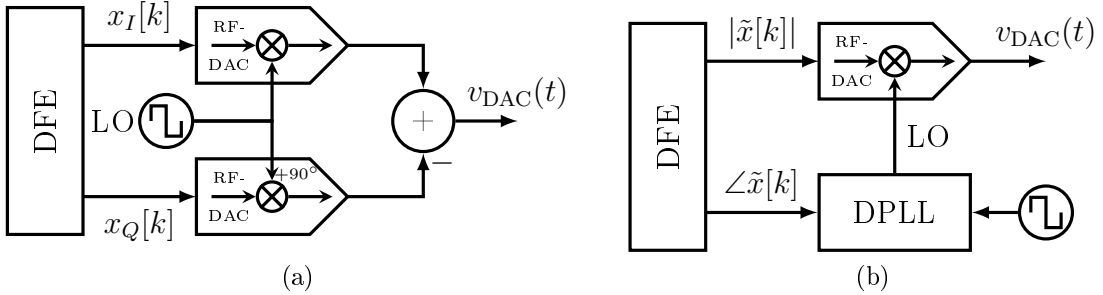
Figure 2.5: Generic CMOS RF transmitters utilizing capacitive RF-DAC circuits. (a) Quadrature architecture, (b) Polar architecture.

2.1.4 Signed Operation

Independent of the chosen architecture, negative amplitude realization is crucial to all capacitive RF-DAC structures. In the polar architecture, the wanted output phasor is generated by the combination of the output voltage magnitude, and the respective phase, where the voltage amplitude is determined by the magnitude of the input code and the phase is modulated on the respective LO signal. Hence, the number of switching cells is $n \geq 0\ \forall t$. The same holds for the MP-SCPA. However, the limiting factor of polar architectures for increasing the signal bandwidth is the achievable bandwidth of the dynamic phase modulation of the LO signal by the DPLL [3]. Nevertheless, a direct approach, where half of the cells are used as virtual ground result in severe power and efficiency drawbacks. To increase the signal bandwidth while keeping the same power and efficiency, the so-called signed polar operation was introduced by Fulde et al. [4, 43]. A sign change of the input code is converted to a 180° phase shift of the LO signal according to $c\,e^{i\phi} = -c\,e^{i(\phi+\pi)}$. For LO signals with 50 % duty cycle this results in an inversion and can be achieved by

using an XOR gate with a dedicated sign bit of the input code. The quadrature LO signals possess a fixed phase as described above. With that, only the first quadrant in the complex plane could be addressed. By inverting the quadrature LO signals for negative in-phase and quadrature input codes, respectively, also the quadrature capacitive RF-DAC can be used in all quadrants of the complex plain efficiently. The drawback of the sign change is the change of the effective sampling point when inverting the LO signal [49]. This can be compensated by linear interpolation of the two consecutive data samples but requires additional digital signal processing operations to achieve a perfect timing of the data sample and the respective LO signal edge [50].

2.1.5 Origins of Nonlinear Effects

The capacitive RF-DAC suffers from various nonlinear effects, originating from internal or external sources. General root causes are, as for all real circuits, mismatch and process variations. The fundamental concept of capacitor mismatch in the cell array and a respective simulation method is discussed in Section 3.4.1. For further details on the implementation and prevention the reader is referred to the literature [3–5, 30, 31, 37, 51, 52].

Furthermore, internal nonidealities arise from misalignment of the sampling instant between data and the respective LO signals or nonideal sign operation, increasing the noise floor and generating unwanted spurs in the output signal [49]. Similar effects are generated due to mismatch in the cell switching times due to the different length of the LO signal distribution into the individual cells.

Another origin of nonlinear effects results from the mismatch of the respective PMOS and NMOS on-resistances of the driving inverters in each switching cell. Unequal on-resistances change the charging and discharging time constant of the cell array, resulting in a code dependent modulation of the output phase, causing AM-PM [30] distortion. Further details are discussed in Section 3.3.3.

External contributors to the nonideal behavior of the capacitive RF-DAC are the (D)PLL and the supply network. Long term clock jitter and the corresponding phase noise of the PLL contribute directly to the output of the RF-DAC, increasing the out-of-band noise floor, see Section 3.4.2. Furthermore, as mentioned above, polar and multiphase architectures rely on the dynamic (resolution) of the DPLL to achieve the required bandwidth of the modulated digital input signal.

One of the main contributors to nonlinear effects is the supply of the capacitive RF-DAC. The supply voltage V_{DD} is also the reference for the digital to analog conversion. Variations of the supply change the reference, corrupting the digital to analog conversion, hence significantly degrading the performance of the capacitive RF-DAC. The output voltage magnitude is then additionally modulated by the variation of V_{DD} as indicated in (2.6). Typically, dedicated low-dropout (LDO) regulators are required to maintain a stable supply voltage over a wide frequency range [4]. Another possibility is to use digital predistortion (DPD) to suppress the effects of the supply voltage variation on the output signal, preserving the linearity

of the capacitive RF-DAC. Degradation of the RF-DAC's performance and a novel concept for a dedicated DPD are discussed in Chapter 4, respectively.

2.2 Digital Predistortion and Nonlinear System Modeling

There is a tradeoff in the design of RF-PAs, either designing for high linearity and sacrificing efficiency or vice versa, as already discussed in Section 1.1. However, systems, especially mobile clients, require both. Furthermore, also a high gain is required such that the signal can be transmitted over long distances. Hence, there is always a compromise in deciding which kind of RF-PA architecture is used [53]. Furthermore, with increasing bandwidth of the baseband signal and higher carrier frequencies, also frequency-dependent effects, i.e. memory effects, become more and more critical. Hence, linearization using DPD is an attractive approach.

This section addresses the fundamentals of digital predistortion and nonlinear system modeling for communication systems. After a brief introduction of the DPD concept, individual characteristics such as model identification are presented. Furthermore, the section reviews the most important mathematical approaches for nonlinear (PA) modeling. Memoryless as well as models with memory, able to include frequency-dependent effects, are discussed.

2.2.1 Concept of Digital Predistortion

The fundamental concept of (digital) predistortion is based on placing a nonlinear component in front of a nonlinear RF-PA such that the combined input-output relation results in a linear gain [10]. The principle is sketched in Figure 2.6, where the nonlinear predistortion gain, combined with the RF-PA linearizes the total gain up to the point of saturation, i.e. when the output power of the RF-PA cannot increase anymore. If the PA input-output characteristic $F : x(t) \rightarrow y(t)$ is modeled by a polynomial function

$$y(t) = F\{x(t)\} = \sum_{j=1}^{J} a_j \cdot x^j(t), \qquad (2.23)$$

then $a_1 \cdot x(t)$ equals the desired linear gain of the system. All higher order terms $a_j \cdot x^j(t)$ for $j = 2, \ldots, J$ represent undesired components, generated by the nonlinear behavior. Hence, a respective DPD $F_{\text{DPD}} : x(t) \rightarrow v(t)$ should modulate the input signal such that the remaining components of the output signal, i.e.

$$y(t) = F\{v(t)\} = F\{F_{\text{DPD}}\{x(t)\}\}, \qquad (2.24)$$

are reduced to the desired linear gain

$$y(t) = a_1 \cdot x(t). \qquad (2.25)$$
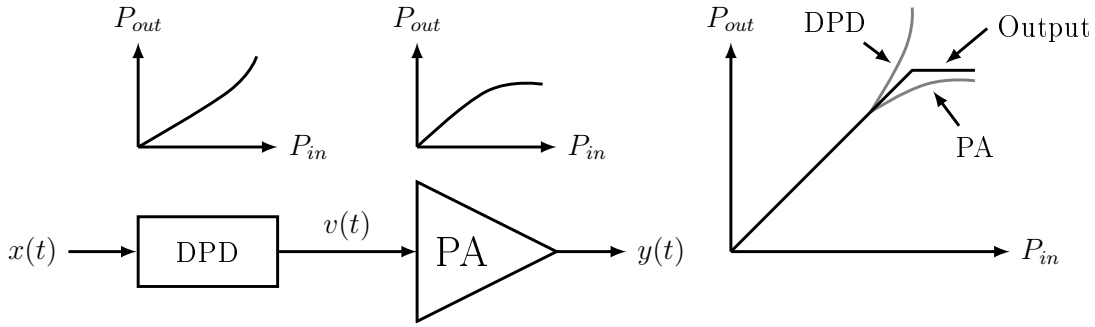
Figure 2.6: Concept of power amplifier linearization with DPD.

The effect of predistortion on the input and output signals in the frequency domain is sketched in Figure 2.7. At the left hand side, the (ideal) input signal $x(t)$ is directly fed to the PA. Due to the nonlinear characteristic, spectral regrowth is introduced, which creates spectral components outside the desired signal spectrum. On the right-hand side, the input is first modulated by the DPD, adding frequency components of the PA's intermodulation products to the input signal appropriately such that the effects on the PA's output are canceled. Henceforth, the spectral regrowth can be eliminated by employing signal processing techniques. Note that the DPD also corrects for in-band distortions, which is not depicted in Figure 2.7.
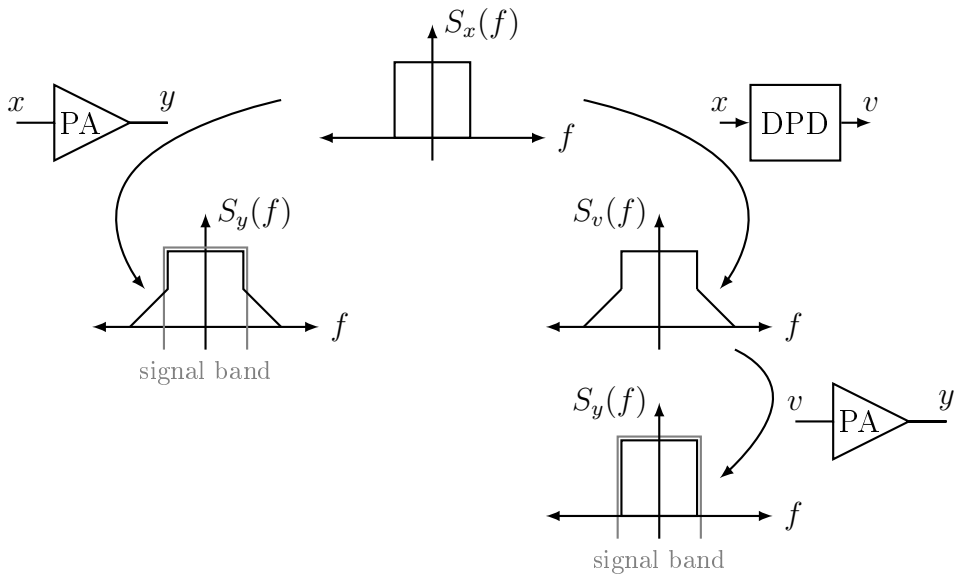
Figure 2.7: Concept of power amplifier linearization in the frequency domain.

DPD also has drawbacks, or better expressed: introducing a predistoriton introduces dedicated requirements for the DSP. First, as indicated in Figure 2.6, the input signal to the RF-PA is amplified in the compression region of the RF-PA, thus causing higher amplitudes of the input signal. However, the maximum output power is not increased. DPD helps to increase the linear output power range

of the overall system. At some point, the RF-PA's output amplitude is limited by other (external) reasons, such as available supply voltage etc., and thus starts clipping, resulting again in nonlinear operation. Henceforth, the DPD must not drive the RF-PA into clipping. Moreover, the enlarged gain for input amplitudes near the compression region of the RF-PA inherently increases the PAPR of the input signal, which needs to be considered in the RF-PA design. Furthermore, as shown in Figure 2.7, the bandwidth of the input signal is increased. Therefore, the oversampling ratio of the baseband signal must be higher than in the non-DPD case to avoid aliasing. This also holds for the coefficient estimation algorithms and the respective feedback path. In integrated circuits, the DPD and the coefficient estimation algorithms must also be implemented on the chip, hence increasing area and power in the digital part. Moreover, a dedicated feedback receiver is typically implemented, capturing the PA's output signal, which is required for coefficient training.

The performance of digital predistortion systems is fundamentally based on the underlying nonlinear system model used in the DPD and the accuracy of the parameter estimation. In the following, the commonly used nonlinear system models in the DPD community are presented and discussed.

2.2.2 Nonlinear System Models

Models of nonlinear systems such as power amplifiers are classified into memoryless models and models with memory. Memoryless models treat the RF-PA's nonlinear behavior as static. Pure memoryless (instantaneous) models are restricted to amplitude distortions only, i. e. the input-output relation depends only on a nonlinear mapping of the output amplitude based on the input signal's magnitude. Models, including phase distortions, are considered to be quasi-memoryless. However, similar to the amplitude distortion, also phase distortions are typically only dependent on the input signal's magnitude. All these arguments are typically referred if the output of the PA is only considered around the carrier frequency, i. e. in the so-called first zone, which is described below.

The performance in terms of modeling accuracy and DPD of (quasi-)memoryless models is very limited, especially if RF-PA's are excited with wideband signals, i. e. 20 MHz and higher [8, 10, 35]. Electrical and thermo-electrical effects generate memory effects [11, 35]. These memory effects introduce frequency dependent dynamics, which cannot be covered by quasi-memoryless models. Due to this limitation, models including memory components such as FIR filters have been introduced to RF-PA modeling. One of the most sophisticated mathematical models is the so-called Volterra series, introduced by Vito Volterra [54] and adapted to nonlinear system modeling by Norbert Wiener [55]. The Volterra series, though very complex, allows to model frequency dependent memory effects of RF-PA's and has also been used for DPD concepts.

Narrowband Approximation

The narrowband approximation, i. e. the modeling of the RF-PA's nonlinearity with equivalent baseband signals, is one of the fundamental concepts of digital predistortion. The narrowband approximation can be used if the input signal's bandwidth is small compared to the carrier frequency. Then, the modeling, simulation, and DPD concentrate only on the resulting nonlinear effects of the envelope of the RF signal around the carrier frequency. For the mathematical analysis, a virtual zonal filter is introduced, perfectly suppressing all spectral signal components except frequencies $f_c \pm f_{\mathrm{SR}}$ [9,35,56], as sketched in Figure 2.8. f_{SR} specifies the band of interest, including the in-band signal and the resulting spectral regrowth of the nonlinear RF-PA, which has to be considered in the modeling and the DPD. This so-called zonal filter is an ideal bandpass filter, placed after the RF-PA. On-chip, digital predistortion systems inherently implement zonal filters in the down-conversion (mixer) and the quadrature demodulator in the feedback receiver.
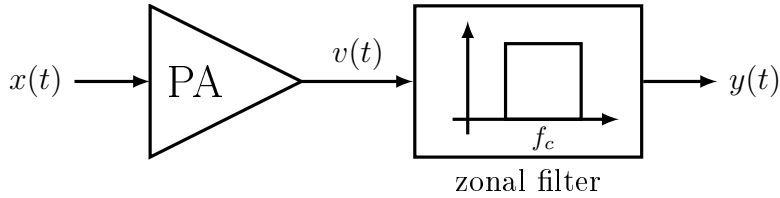
Figure 2.8: Concept of placing a zonal filter, i. e. an ideal bandpass filter, after the PA such that only signal components around the carrier frequency f_c remain.

Similar to the passband representation, the output of the RF-PA can be also represented by an equivalent complex baseband signal

$$
\begin{aligned}
y(t) &= \mathrm{Re}\left\{ \tilde{y}(t)\, e^{j\,2\pi\, f_c\, t} \right\} \\
&= y_A(t)\, \cos\left[2\pi\, f_c\, t + \vartheta\,(t) \right],
\end{aligned}
\tag{2.26}
$$

where

$$
\tilde{y}(t) = y_A(t)\, e^{j\,\vartheta(t)}.
\tag{2.27}
$$

$y_A(t)$ and $\vartheta\,(t)$ are the output envelope and phase of the RF-PA, respectively. Let us assume that there is a zonal filter placed after the RF-PA, i. e. no higher order harmonics at multiples of the carrier frequency are present. The relation between the so-defined baseband signal $\tilde{y}(t)$ and the equivalent baseband input signal $\tilde{x}(t)$ shall be modeled by $\tilde{F}$, such that

$$
\tilde{y}(t) = \tilde{F}\left\{ \tilde{x}(t) \right\},
\tag{2.28a}
$$

where $\tilde{y}(t)$ represents the equivalent baseband signal of the RF-PA output, only including the down-converted output signal in the first zone. Conclusively, different models, or at least different parameters, are required when only considering the equivalent baseband signals, i. e. $\tilde{F}\left\{ \cdot \right\} \neq F\left\{ \cdot \right\}$ [11]. In the following, nonlinear

models for passband as well as baseband signals and systems are discussed, where $\tilde{\cdot}$ always denotes the equivalent baseband representation.

Equivalent baseband models are preferred for system-level simulations, as the required oversampling ratio can be dramatically reduced compared to their RF counterparts. Furthermore, also complicated signal processing algorithms such as the DPD itself and its corresponding coefficient estimation are much easier to implement when using the digital baseband signal samples.

Memoryless and Quasi-Memoryless Nonlinear Models

A memoryless bandpass nonlinearity can be represented by

$$y(t) = F\left[x\left(t\right)\right], \tag{2.29}$$

where $F\left(\cdot\right)$ is a nonlinear function mapping the instantaneous real-valued passband input signal $x(t)$ to the real-valued output signal, i.e. $F : x \to y$, where $x, y \in \mathbb{R}$. The passband input signal $x(t)$ is

$$x(t) = |\tilde{x}(t)| + \cos\left[2\pi f_c t + \varphi(t)\right], \tag{2.30}$$

with

$$|\tilde{x}(t)| = \sqrt{x_I^2(t) + x_Q^2(t)}, \tag{2.31a}$$

$$\varphi(t) = \tan^{-1}\left[\frac{x_Q(t)}{x_I(t)}\right] \tag{2.31b}$$

The term instantaneous indicates that the output at time instance t is solely dependent on the input at time instant t, i.e. the system has no memory. In literature such systems are often referred to not include frequency dependent (dynamic) effects. Although this is true for the system itself, one must consider that the spectral components of the output $y(t)$ are in general different from the input signal $x(t)$.

Memoryless models can only represent envelope nonlinearities [7, 35], i.e.

$$y(t) = f\left[|\tilde{x}(t)|\right] \cos\left(2\pi f_c t + \varphi(t)\right), \tag{2.32}$$

where $y(t)$ represents only the first zone using the narrowband approximation. This phenomenon is called amplitude distortion and typically referred to as AM-AM. Hence, (2.38) is also called a strictly-memoryless or instantaneous model. In this work, the term memoryless is used to indicate a strictly-memoryless model.

Nevertheless, typically power amplifiers also introduce a nonlinear phase shift depending on the input signal amplitude, which is called AM-PM distortion or AM-PM conversion. Hence, the analytical concept of (2.32) must be extended. In general, such a passband system can be described by

$$y(t) = f\left[|\tilde{x}(t)|\right] \cos\left(2\pi f_c t + \varphi(t) + g\left[|\tilde{x}(t)|\right]\right), \tag{2.33}$$

where $f\left[|\tilde{x}(t)|\right]$ is the envelope nonlinearity and $g\left[|\tilde{x}(t)|\right]$ the phase nonlinearity, i.e. the AM-AM and AM-PM, respectively. Note that (2.33) describes the input-output function directly for bandpass signals/systems assuming a zonal filter. Although $f\left[|\tilde{x}(t)|\right]$ and $g\left[|\tilde{x}(t)|\right]$ are both considered to be instantaneous nonlinearities, (2.33) is referred to as a quasi-memoryless model due to the fact that the envelope and the phase are nonlinearly dependent on the input signal.

For system level simulations and digital predistortion, however, it is usually preferred to use the equivalent complex baseband representation. The equivalent baseband representation of (2.33) is given by

$$\tilde{y}(t) = f\left[|\tilde{x}(t)|\right] \, e^{i\,g[|\tilde{x}(t)|]} \, e^{i\,\varphi(t)}, \tag{2.34}$$

where

$$\begin{aligned} y(t) &= \mathrm{Re}\left\{\tilde{y}(t)\, e^{i\,2\pi f_c t}\right\} \\ &= \mathrm{Re}\left\{f\left[|\tilde{x}(t)|\right]\, e^{i\,\varphi(t)+i\,g[|\tilde{x}(t)|]}\, e^{i\,2\pi f_c t}\right\}. \end{aligned} \tag{2.35}$$

Alternatively, (2.34) can also be represented in quadrature form [8]

$$y_I(t) = f\left[|\tilde{x}(t)|\right]\, \cos\left(g\left[|\tilde{x}(t)|\right] + \varphi(t)\right), \tag{2.36a}$$

$$y_Q(t) = f\left[|\tilde{x}(t)|\right]\, \sin\left(g\left[|\tilde{x}(t)|\right] + \varphi(t)\right). \tag{2.36b}$$

Figure 2.9a and Figure 2.9b show the modeling of nonlinear effects for the polar and the quadrature form of the equivalent complex baseband signal, respectively.

One possible memoryless passband model is the Taylor (power) series [8]

$$y(t) = F\left[x\left(t\right)\right] = \sum_{j=1}^{\infty} \alpha_j\, x^j(t), \tag{2.37}$$

where for practical system modeling and simulation, (2.37) is limited to J exponential terms

$$y(t) = F\left[x\left(t\right)\right] \cong \sum_{j=1}^{J} \alpha_j\, x^j(t), \tag{2.38}$$

which is referred to as a memoryless passband polynomial model [57, 58]. In general, a system representation as in (2.37) and (2.38) is referred to as an analytical model and can be used to describe effects of nonlinear systems such as intermodulation, cross-modulation, compression, and desensitization with closed-form equations as already discussed in Section 1.2.

The complex baseband equivalent model of the polynomial model is given by [7, 57, 59]

$$\tilde{y}(t) = \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \tilde{\alpha}_j\, \tilde{x}(t)\, |\tilde{x}(t)|^{j-1}, \tag{2.39}$$

(a)

(b)
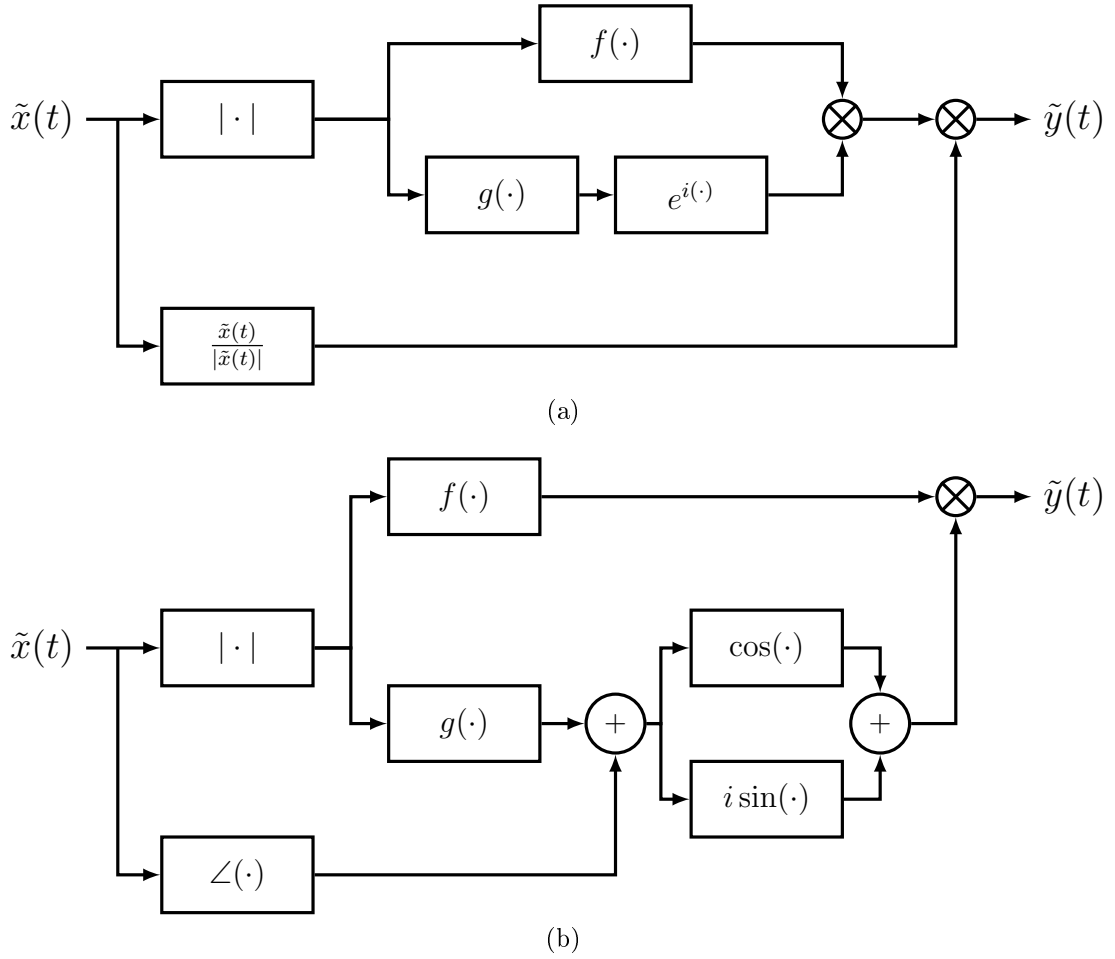
Figure 2.9: Nonlinear quasi-memoryless model for (a) the polar and (b) the quadrature form of the equivalent baseband signal, respectively.

where

$$\tilde{\alpha}_j = \alpha_j \, \frac{1}{2^{j-1}} \begin{pmatrix} j \\ \frac{j-1}{2} \end{pmatrix}. \tag{2.40}$$

Similar to the passband model (2.38), the equivalent baseband model (2.39) is a strictly memoryless model if all coefficients $\tilde{\alpha}_j$ are real-valued [58]. The equivalent baseband model only includes the odd-order terms as only these terms generate distortions in the first zone as shown in the following. The passband input signal of the RF-PA is

$$\begin{aligned} x(t) &= \mathrm{Re}\left\{ |\tilde{x}(t)| \; e^{i\,\varphi(t)} \, e^{i\,\omega_c t} \right\} \\ &= \mathrm{Re}\left\{ \tilde{x}(t) \, e^{i\,\omega_c t} \right\} \\ &= \frac{1}{2} \left[\tilde{x}(t) \, e^{i\,\omega_c t} + \tilde{x}^*(t) \, e^{-i\,\omega_c t} \right]. \end{aligned} \tag{2.41}$$

Substituting (2.41) into the passband polynomial model (2.38) yields

$$y(t) = \sum_{j=1}^{J} a_j \, \frac{1}{2^j} \left[\tilde{x}(t) \, e^{i\,\omega_c t} + \tilde{x}^*(t) \, e^{-i\,\omega_c t} \right]^j. \tag{2.42}$$

Concentrating only on the power series of the terms inside the brackets and omitting (t) for better readability, gives

$$j = 1 : \tilde{x} \, e^{i\,\omega_c t} + \tilde{x}^* \, e^{-i\,\omega_c t} \tag{2.43a}$$

$$j = 2 : \tilde{x}^2 \, e^{i\,2\omega_c t} + \tilde{x}^{*2} \, e^{-i\,2\omega_c t} + 2\,\tilde{x}\,\tilde{x}^* \tag{2.43b}$$

$$j = 3 : \tilde{x}^3 \, e^{i\,3\omega_c t} + \tilde{x}^{*3} \, e^{-i\,3\omega_c t} + 3\,\tilde{x}^2\,\tilde{x}^* \, e^{i(2\omega_c t - \omega_c t)} + 3\,\tilde{x}\,\tilde{x}^{*2} \, e^{i(\omega_c t - 2\omega_c t)} \tag{2.43c}$$

$$j = 4 : \tilde{x}^4 \, e^{i\,2\omega_c t} + \tilde{x}^{*4} \, e^{-i\,2\omega_c t} + 4\,\tilde{x}^3\,\tilde{x}^* \, e^{i(3\omega_c t - \omega_c t)}$$
$$+ 4\,\tilde{x}\,\tilde{x}^{*3} \, e^{i(\omega_c t - 3\omega_c t)} + 6\,\tilde{x}\,\tilde{x}^* \tag{2.43d}$$

$$j = 5 : \tilde{x}^5 \, e^{i\,5\omega_c t} + \tilde{x}^{*5} \, e^{-i\,5\omega_c t} + 5\,\tilde{x}^4\,\tilde{x}^* \, e^{i(4\omega_c t - \omega_c t)} + 5\,\tilde{x}\,\tilde{x}^{*4} \, e^{i(\omega_c t - 4\omega_c t)}$$
$$+ 10\,\tilde{x}^3\,\tilde{x}^{*2} \, e^{i(3\omega_c t - 2\omega_c t)} + 10\,\tilde{x}^2\,\tilde{x}^{*3} \, e^{i(2\omega_c t - 3\omega_c t)} \tag{2.43e}$$

Only odd-order terms result in distortions in the first zone of the RF-PA output, i.e. when the exponential is $e^{\pm i\,\omega_c t}$. Moreover, only combinations of $\tilde{x}^j\,\tilde{x}^{*l}$ with $|j - l| = 1$ contribute to the the first zone. Henceforth, by using the results of (2.43), and assuming again a zonal filter, the output of the RF-PA around the carrier follows to

$$y(t) = \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \alpha_j \, \frac{1}{2^j} \binom{j}{\frac{j-1}{2}} \left[\tilde{x}(t) \, |x(t)|^{j-1} \, e^{i\,\omega_c t} + \tilde{x}^*(t) \, |x(t)|^{j-1} \, e^{-i\,\omega_c t} \right]. \tag{2.44}$$

Finally, the equivalent baseband signal is given by

$$\tilde{y}(t) = \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \tilde{\alpha}_j \, \tilde{x}(t) \, |\tilde{x}(t)|^{j-1}, \tag{2.45}$$

with coefficients $\tilde{\alpha}_j$ as in (2.40), showing that only odd-order terms of the passband polynomial model (2.38) contribute to the nonlinearity of the baseband output signal $\tilde{y}(t)$.

The memoryless passband polynomial model (2.38) can be extended to a quasi-memoryless model by introducing a second instantaneous nonlinearity for the quadrature component [58]

$$y(t) = \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \alpha_j \, x_I^j(t) - \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \beta_j \, x_Q^j(t), \tag{2.46}$$

where

$$x_I = \text{Re} \left\{ \tilde{x}(t) \, e^{\omega_c t} \right\} \tag{2.47a}$$

$$x_Q = \text{Im} \left\{ \tilde{x}(t) \, e^{\omega_c t} \right\} \tag{2.47b}$$

$$\tag{2.47c}$$

The equivalent baseband model is similar to the memoryless model

$$\tilde{y}(t) = \sum_{\substack{j=1 \\ j \text{ is odd}}}^{J} \tilde{\gamma}_j \, \tilde{x}(t) \, |\tilde{x}(t)|^{j-1}, \tag{2.48}$$

but with complex-valued coefficient $\tilde{\gamma}_j \in \mathbb{C}$

$$\tilde{\gamma}_j = (\alpha_j + i \, \beta_j) \, \frac{1}{2^{j-1}} \binom{j}{\frac{j-1}{2}}. \tag{2.49}$$

The memoryless and quasi-memoryless polynomial models derived above only include odd-order terms. Nevertheless, Enzinger et al. [58, 60] introduced the mathematical justification of even-order terms in baseband polynomial models for RF-PA modeling and predistortion, resulting in better performance for modeling and DPD. The transformation pair for the quasi-memoryless passband and equivalent baseband model, including non-zero even-order terms, are given by

$$y(t) = \sum_{j \in J} \alpha_j \, x_I(t) \, |x_I(t)|^{j-1} - \sum_{j \in J} \beta_j \, x_Q(t) \, |x_Q(t)|^{j-1} \tag{2.50a}$$

$$\tilde{y}(t) = \sum_{j \in J} \tilde{\gamma}_j \, \tilde{x}(t) \, |\tilde{x}(t)|^{j-1} \tag{2.50b}$$

with

$$\tilde{\gamma}_j = (\alpha_j + i \, \beta_j) \, \frac{2}{\sqrt{\pi}} \frac{\Gamma \left(\frac{j+2}{2} \right)}{\Gamma \left(\frac{j+3}{2} \right)}. \tag{2.51}$$

Other approaches for AM-AM and AM-PM modeling include, but are not limited to, the Saleh and the Rapp model [61, 62]. In contrast to the polynomial and power series approach, these kind of models are based on parametrized nonlinear functions.

The Saleh model was introduced to model traveling-wave-tube (TWT) amplifiers, but also finds its use (sometimes extended) for semiconductor based RF-PAs modeling and predistortion [63–65]. The AM-AM and AM-PM functions for an equivalent complex input signal $\tilde{x}(t) = |\tilde{x}(t)| \exp \left[i \, \phi(t) \right]$ are defined as

$$f \left(|\tilde{x}(t)| \right) = \frac{\alpha_a \, |\tilde{x}(t)|}{1 + \beta_a \, |\tilde{x}(t)|^2}, \tag{2.52a}$$

$$g \left(|\tilde{x}(t)| \right) = \frac{\alpha_\phi \, |\tilde{x}(t)|^2}{1 + \beta_\phi \, |\tilde{x}(t)|^2}. \tag{2.52b}$$

Parameters $\alpha_{a/\phi}$ and $\beta_{a/\phi}$ must be determined to fit the model to the dedicated RF-PA. Rearranging (2.52a) and (2.53b) allows to use linear estimation algorithms [9]. Figure 2.10a shows the AM-AM and AM-PM characteristic of a representative nonlinear RF-PA. The Saleh model can also be represented in quadrature form [35]:

$$f_I\left(|\tilde{x}(t)|\right) = \frac{\alpha_I\,|\tilde{x}(t)|}{1 + \beta_I\,|\tilde{x}(t)|^2}, \tag{2.53a}$$

$$f_Q\left(|\tilde{x}(t)|\right) = \frac{\alpha_Q\,|\tilde{x}(t)|^3}{\left(1 + \beta_Q\,|\tilde{x}(t)|^2\right)^2}. \tag{2.53b}$$

The Saleh model does not represent a hard limit function, i.e. the output power starts to drop after a peak, even if the input power further increases. Models incorporating a "hard" clipping behavior are the Rapp and the Cann model.

The Rapp model is used to emulate solid state RF-PAs with a smooth transition from the linear region to the saturation region [66]. The AM-AM and AM-PM equations are respectively given by

$$f\left(|\tilde{x}(t)|\right) = \frac{\alpha_0\,|\tilde{x}(t)|}{\left[1 + \left(\frac{|\tilde{x}(t)|}{x_{\mathrm{sat}}}\right)^{2p}\right]^{\frac{1}{2p}}}, \tag{2.54a}$$

$$g\left(|\tilde{x}(t)|\right) \approx 0, \tag{2.54b}$$

with $p > 0$ defining the smoothness from the linear to the limiting region, x_{sat} representing the limiting output amplitude, and α_0 is the small signal gain. The AM-PM is assumed to be negligible [62]. While this is quite optimistic, also for solid state power amplifiers, it still proves to be useful for modeling nonlinear systems, especially for input signals with small bandwidths. The nonlinear characteristic of (2.54a) for different values of p is shown in Figure 2.10b.

Nonlinear Models with Memory - The Volterra Series

All quasi-memoryless models described above assume that the nonlinear function, i.e. the mapping of current input sample to current output sample, also holds for modulated input signals, i.e. $F(x) \rightarrow F\{x(t)\}$. This is not true in general, but may be sufficient if the bandwidth of the modulated input signal is small enough compared to the inherent bandwidth of the nonlinear system itself, validated by the vast usage of these models in practical transmitter systems and publications. However, for input signals, which occupy a larger bandwidth, these quasi-memoryless models are not sufficient to predict the effect on the output signal. Nowadays communication standards such as Wi-Fi 6 (IEEE802.11ax) allow for baseband bandwidths of up to $160\,\mathrm{MHz}$. Furthermore, the OFDM based modulation schemes possess an inherent high crest factor of $11 - 14\,\mathrm{dB}$. Such signal characteristics give rise to a frequency-dependent behavior. This nonlinear frequency dependent behavior is referred to as memory effects. Representative in the
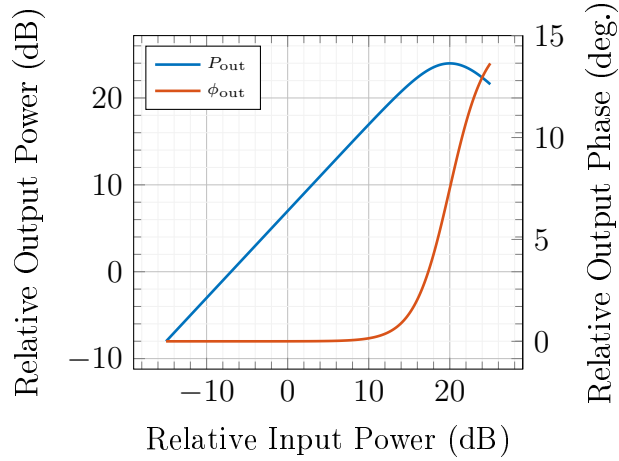
(a)   AM-AM and AM-PM, Saleh's model.
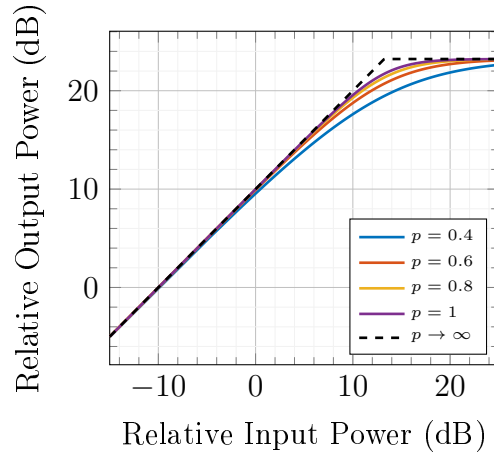
(b)   AM-AM, Rapp model for different sharpness factors p, $\alpha_0 = 1$, and $P_\text{sat} = 21\,\text{dB}$

Figure 2.10: Representative AM-AM and AM-PM characteristics of (quasi-) memoryless nonlinear system models.

time domain, not only the instantaneous input signal sample at time instance t but also previous samples affect the current output sample, as briefly sketched in Figure 2.11. Henceforth, the quasi-memoryless models reach their limit in terms of modeling and are thus insufficient for advanced predistortion approaches. As a result, the models must be extended, such that memory effects can be characterized, leading to mathematical descriptions with higher complexity. Examples are the Volterra series, the Wiener model, the Hammerstein model, and the memory polynomials, described below.

The Volterra series is one of the fundamental and widely studied mathematical concepts to describe nonlinear systems such as power amplifiers with fading memory [9, 26, 54, 55]. Fading memory requires the system to forget at some point in
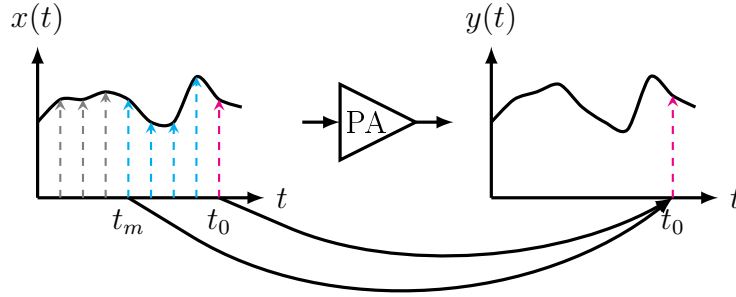
Figure 2.11: The output sample $y(t_0)$ depends not just on $x(t_0)$, but also on the previous m samples.

time, i. e. it is causal and input signals after a time $(t-t_M)$ for $t_M < \infty$ do not contribute to the output anymore [67]. In general, the Volterra series is an extension to the Taylor series (2.37) with memory. The memory of the system is introduced by multi-dimensional convolutions with impulse responses corresponding to the p-th order. The Volterra series is defined by [57]

$$y(t) = \sum_{p=1}^{\infty} \int \cdots \int h_p(\boldsymbol{\tau_p}) \prod_{j=1}^{p} x(t - \tau_j) \, d\boldsymbol{\tau_p}, \qquad (2.55)$$

with $\boldsymbol{\tau_p} = [\tau_1, \tau_2, \ldots, \tau_p]$, $d\boldsymbol{\tau_p} = d\tau_1 \cdot d\tau_2 \cdots d\tau_p$, h_0 is a constant, and $h_p(\cdot)$ for $p \geq 1$ is the p-th-order Volterra kernel. Similar as an impulse response characterizes an LTI system, a nonlinear system, which can be described by the Volterra series, is characterized by the respective Volterra kernels [35]. An intuitive example is shown in Appendix A.1. For analytical considerations, and without loss of generality, the kernels are assumed to be symmetric, i. e. the p-th kernel $h_p(\tau_1, \tau_2, \ldots, \tau_p)$ is independent on the $n!$ possible sequences of its arguments [26]. For example, $h_2(\tau_1, \tau_2) = h_2(\tau_2, \tau_1)$. Another possibility, which is also often used in literature, of expressing (2.55) is

$$y(t) = H_1[x(t)] + H_2[x(t)] + \cdots + H_p[x(t)], \qquad (2.56)$$

with the p-th-order Volterra operator

$$H_p[x(t)] = \int \cdots \int h_p(\tau_1, \tau_2, \ldots, \tau_p)\, x(t - \tau_1)\, x(t - \tau_2) \cdots x(t - \tau_p)\, d\tau_1\, d\tau_2 \cdots d\tau_p. \qquad (2.57)$$

The Volterra series can't be used to model ideal clipping functions [35]. Nevertheless, Norbert Wiener proposed to use an orthogonal set of functionals, so-called G-functionals, as Volterra kernels to approximate a given nonlinear system [55]. This so-called Wiener theory of nonlinear systems largely extended the applicable nonlinear system modeling by the Volterra series.

The Volterra series in (2.55) is defined for real-valued (bandpass) systems and signals. Inherently, also the Volterra kernels are real-valued functions. Similar to the quasi-memoryless bandpass models above, using (2.55) requires signals and systems to be simulated with sampling rates several times higher than the carrier frequency due to the generation of higher-order intermodulation distortions. This marks passband Volterra models inefficient for complete system-level simulations, and also for DPD purposes.

The complex baseband Volterra series, allowing simulation and modeling with complex baseband signals, was first derived by Bendetto et al. in [68]. Using the narrowband approximation, as discussed above, it can be shown that only odd-order terms contribute to the output in the first zone [10, 26]. The Volterra series for baseband systems is given by [7, 9, 11]

$$\tilde{y}(t) = \sum_{p=1}^{P} \int \cdots \int \tilde{h}_{2p+1}\left(\boldsymbol{\tau}_{2p+1}\right)$$
$$\times \prod_{i=1}^{p+1} \tilde{x}(t - \tau_i) \prod_{i=p+2}^{2p+1} \tilde{x}^*(t - \tau_i)\, d\boldsymbol{\tau}_{2p+1}, \qquad (2.58)$$

with

$$\tilde{h}\left(\boldsymbol{t}_{2p+1}\right) = \left(\frac{1}{2}\right)^{2p} \binom{2p+1}{p} h_{2p+1}\left(\boldsymbol{t}_{2p+1}\right)$$
$$\times \exp\left[-i\,2\pi\,f_0\left(\sum_{i=1}^{p+1} t_i - \sum_{i=p+2}^{2p+1} t_i\right)\right], \qquad (2.59)$$

where $h\left(t_1, t_2, \ldots, t_{2p+1}\right)$ is the real-valued $2p+1$ kernel of the passband model (2.55).

For digital (baseband) predistortion, the Volterra series must be represented by discrete samples. Henceforth, the p-dimensional continuous convolutions above are replaced by discrete time convolutions. The discrete time Volterra series is given by [7, 35]

$$y[k] = \sum_{p=1}^{P-1} \sum_{m_1=0}^{M-1} \cdots \sum_{m_p=m_{2p+1}}^{M-1} \tilde{h}_{2p+1}\left[\boldsymbol{m}_{2p+1}\right] \prod_{i=1}^{p+1} \tilde{x}[k - m_i] \prod_{i=p+2}^{2p+1} \tilde{x}^*[k - m_i] \quad (2.60)$$

with the kernels given by

$$\tilde{h}_{2p+1}\left[\boldsymbol{k}_{2p+1}\right] = \tilde{h}\left(\boldsymbol{k}_{2p+1}\, T_s\right). \qquad (2.61)$$

The continuous-time signal $\tilde{y}(t)$ can be reproduced by the samples of the discrete-time Volterra series at $t = k\,T_s$ [9, 69] using the kernels as defined in (2.61), i.e. $\tilde{y}(k\,T_s) = \tilde{y}[k]$.

Wiener, Hammerstein, and Memory Polynomial Models

Models based on the Volterra series have been proven to be very accurate in nonlinear systems modeling. However, in terms of predistortion, these functions are rather complex to be implemented. So-called pruned Volterra models limit the number and complexity of the base functions used, i. e. the Volterra kernels. The Wiener and Hammerstein models represent a simplified form of the general Volterra series, reducing accuracy but being more implementation friendly for DPD purposes. Both are composed of a combination of a static nonlinearity and a digital filter as shown in Figure 2.12, where typically digital FIR filters are preferred. The Wiener model consists of a digital filter $H(z)$ followed by a static nonlinear function $g(\cdot)$. The simplified Hammerstein model, i. e. the two-dimensional case, is represented by a static nonlinear function followed by a digital filter.

If the static nonlinearity is modeled by a J-order polynomial, and an M-tap FIR filter is used, then the output of the Wiener model is given by

$$y_{\mathrm{W}}[k] = \sum_{j=1}^{J} g_j \cdot \left[\sum_{m=0}^{M-1} h_m \cdot x\left[k-m\right] \right]^{j}. \tag{2.62}$$

One possible equivalent baseband model using (2.50b) as the static nonlinear function, is given by

$$\tilde{v}[k] = \sum_{m=0}^{M-1} \tilde{h}_m \cdot \tilde{x}[k-m], \tag{2.63a}$$

$$\tilde{y}_{\mathrm{W}}[k] = \sum_{j=1}^{J} \tilde{g}_j \, \tilde{v}[k] \, |\tilde{v}[k]|^{j-1}$$

$$= \sum_{j=1}^{J} \tilde{g}_j \cdot \left[\sum_{m=0}^{M-1} \tilde{h}_m \cdot \tilde{x}[k-m] \right] \cdot \left| \sum_{m=0}^{M-1} \tilde{h}_m \cdot \tilde{x}[k-m] \right|^{j-1}. \tag{2.63b}$$

Unfortunately, the Wiener model is only partially linear in its parameters and thus requires more complex estimation algorithms. Thus the Wiener model is also less attractive for predistortion approaches [70].

The Hammerstein model, again using a J-order polynomial, and an M-tap FIR filter, is given by

$$y_{\mathrm{H}}[k] = \sum_{m=0}^{M-1} h_m \cdot \sum_{j=1}^{J} g_j \cdot x^{j}\left[k-m\right]. \tag{2.64}$$

Similar as for the Wiener model, one possible model in the equivalent baseband

using (2.50b) is given by

$$\tilde{v}[k] = \sum_{j=1}^{J} \tilde{g}_j \, \tilde{x}[k] \, |\tilde{x}[k]|^{j-1}, \tag{2.65a}$$

$$\tilde{y}_{\mathrm{H}}[k] = \sum_{m=0}^{M-1} \tilde{h}_m \, \tilde{v}[k - m]$$

$$= \sum_{m=0}^{M-1} \tilde{h}_m \cdot \sum_{j=1}^{J} \tilde{g}_j \, \tilde{x}[k - m] \, |\tilde{x}[k - m]|^{j-1}. \tag{2.65b}$$

Equations (2.64) and (2.65b) represent the two-dimensional Hammerstein model, i. e. there is only one FIR filter after the static nonlinearity. Henceforth, there are a total of $M + J$ coefficients. Hammerstein models have been proven to be more effective for DPD than the Wiener model [23, 70]. A way to extend the Hammerstein model is to use different FIR filters for each monomial by combining the filter and the polynomial coefficients to a two-dimensional array with independent parameters $\{a_{jm}\}$. This results in a total of $M \cdot J$ coefficients. The passband and the baseband model from (2.64) and (2.65b), respectively, become

$$y_{\mathrm{GH}}[k] = \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm} \, x^j \, [k - m], \tag{2.66a}$$

$$\tilde{y}_{\mathrm{MP}}[k] = \sum_{j=1}^{J} \sum_{m=0}^{M-1} \tilde{a}_{jm} \, \tilde{x}[k - m] \, |\tilde{x}[k - m]|^{j-1}. \tag{2.66b}$$

(2.66a) is referred to as the general Hammerstein model and (2.66b) represents the so-called memory polynomial (MP) model[1] [71], as shown in shown in Figure 2.12c. With the extension to the general Hammerstein model (2.66a) the output is linear in the parameters a_{jm}. Thus linear estimators can be used. The MP model has been proven as an effective approach to linearize RF-PAs using DPD [24, 72, 73].

An even more sophisticated approach of the memory polynomial, the generalized memory polynomial (GMP), has been introduced by Morgan et al. [21]. The product terms in the MP (2.66b) contain only input samples at the same time instant, whereas the Volterra series suggests considering also product terms with different time shifts. These so-called cross-terms are introduced to the MP by

---

[1] If the static nonlinear function is modeled with the polynomial in (2.50b)
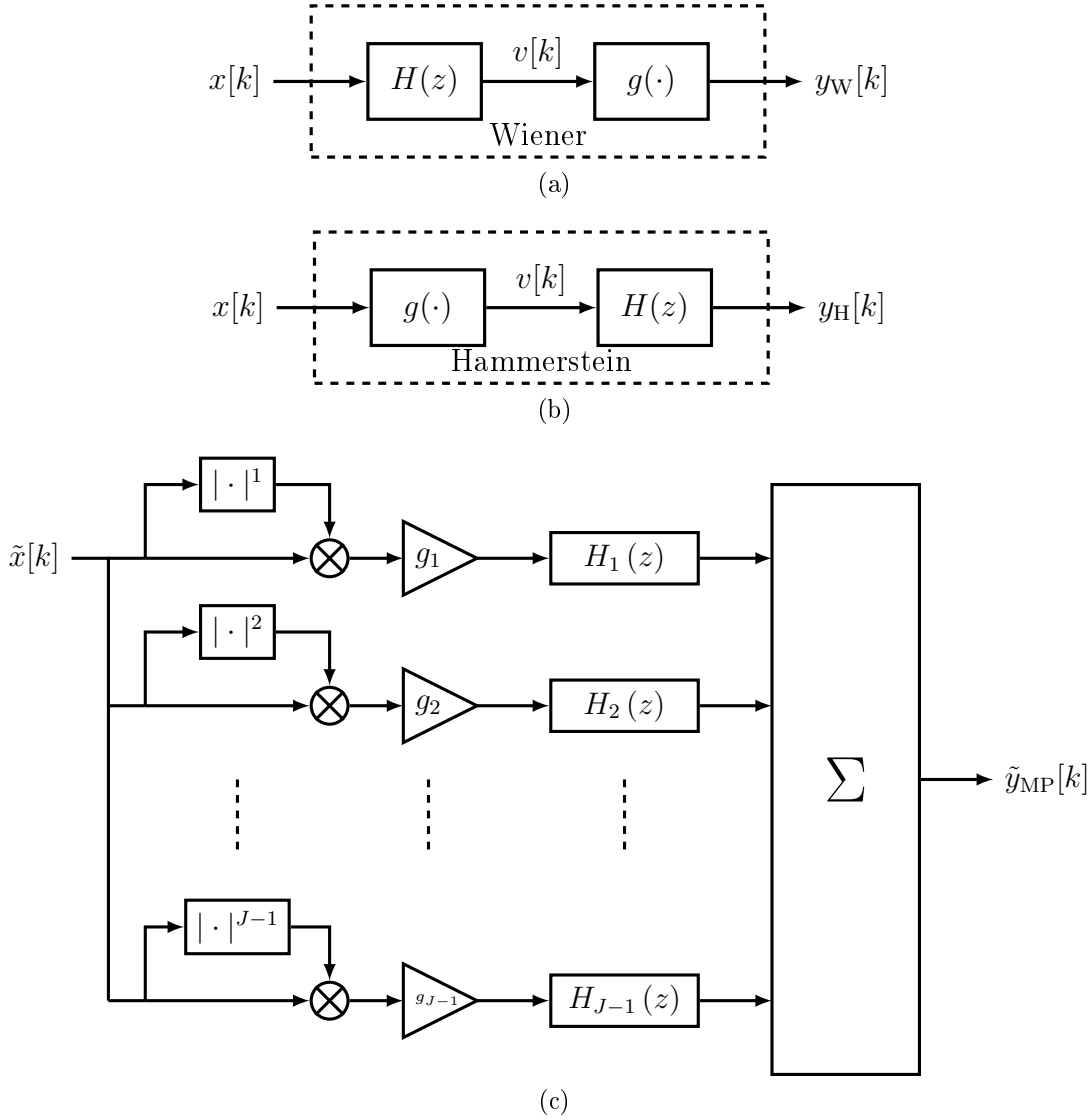
Figure 2.12: Block Diagram of (a) the Wiener model, (b) the Hammerstein model, and (c) the memory polynomial model.

Morgan, where conclusively the GMP is defined as

$$
\begin{aligned}
\tilde{y}_{\text{GMP}}[k] = &\sum_{j=0}^{J_a-1} \sum_{l=0}^{L_a-1} \tilde{a}_{jl}\, \tilde{x}[k-l]\, |\tilde{x}[k-l]|^j \\
&+ \sum_{j=1}^{J_b} \sum_{l=0}^{L_b-1} \sum_{m=1}^{M_b} \tilde{b}_{jlm}\, \tilde{x}[k-l]\, |\tilde{x}[k-l-m]|^j \\
&+ \sum_{j=1}^{J_c} \sum_{l=0}^{L_c-1} \sum_{m=1}^{M_c} \tilde{c}_{jlm}\, \tilde{x}[k-l]\, |\tilde{x}[k-l+m]|^j \,, \qquad (2.67)
\end{aligned}
$$

where J_a and L_a correspond to the aligned signal and envelope, equivalent to the

MP in (2.66b). J_b, L_b, M_b correspond to the number of coefficients for lagging signal envelope. Similar, J_c, L_c, M_c define the number of coefficients for leading signal envelope. All coefficients are linear in the output, which allows to use linear estimation algorithms.

A reduced form of the (generalized) memory polynomial was introduced by Hammi et al. in [74], where the parallel nonlinear filter structure solely depends on the magnitude of the input signal, i. e.

$$\tilde{y}_{\text{EMP}}[k] = x[k] \cdot \sum_{j=1}^{J} \sum_{m=0}^{M-1} \tilde{a}_{jm} \, |\tilde{x}\,[k-m]|^{j-1}. \tag{2.68}$$

Only the last M samples of the input signal's magnitude are considered. Hence, (2.68) is referred to as envelope memory polynomial (EMP). According to Hammi et al., the EMP can be used for passband as well as baseband predistortion systems. Similar to the MP and GMP, the output of the model is linear in coefficients a_{jm}, allowing to use linear estimation algorithms. Though its complexity is reduced, the EMP's DPD performance is in some cases comparable to the MP [34, 74–78]. Comparing (2.68) to the GMP (2.67) shows that the EMP is solely consisting of the lagging cross-terms, i. e. the magnitude always lags the input signal. Intuitively, the memory effects are thus assumed to be dominated by the magnitude of the previous samples. The proposed predistortion concept of this thesis shows similarities to (2.68) and is discussed in Section 4.3.

The derivation of the Volterra series from passband to baseband by Benedetto et al. [68] shows that only odd-order terms produce outputs in the first zone, i. e. at the carrier frequency. Henceforth, even-order terms are often neglected in RF predistortion approaches. However, studies showed that by including even-order terms, results achieved by DPD can be improved [58]. The first mathematical proof was provided by Enzinger [7]. The proposed DPD approach in this thesis, discussed in Chapter 4, also shows the improvement of the DPD if even-order terms are included in the model.

2.2.3 Coefficient Estimation Techniques

There are a lot of different specialized coefficient and model estimation concepts used for DPD systems. This subsection briefly describes the fundamental concepts of identification strategies using linear estimators for the equivalent baseband signals only. Thus the tilde symbol is omitted here. The following discussions about identification methods such as the direct and indirect learning are based on the work of Wood [10].

A preferable and estimation friendly model of an input-output relation of a nonlinear system such as an RF-PA can be represented by a linear model of the form

$$\mathbf{y} = \mathbf{H}\,\boldsymbol{\theta} + \mathbf{n}, \tag{2.69}$$

where $\boldsymbol{\theta}$ is a vector of coefficients, $\mathbf{n}$ is an additive random noise vector, and $\mathbf{H}$ is the observation matrix, which depends on the chosen underlying signal (channel) model. In this case, $\mathbf{y}$ is linear in the parameters $\boldsymbol{\theta}$. However, $\mathbf{H}$ can consist of nonlinear basis functions such as

$$
\begin{aligned}
\mathbf{H} &= [\mathbf{h}_1 \; \mathbf{h}_2 \; \dots \; \mathbf{h}_J] \\
&= \begin{bmatrix}
x^1[k] & x^2[k] & \dots & x^J[k] \\
x^1[k-1] & x^2[k-1] & \dots & x^J[k-1] \\
\vdots & \vdots & \ddots & \dots \\
x^1[k-K+1] & x^2[k-K+1] & \dots & x^J[k-K+1]
\end{bmatrix}
\end{aligned}
\tag{2.70}
$$

where each row represents a polynomial at time index k with corresponding coefficients

$$
\boldsymbol{\theta} = \begin{bmatrix} \theta^0 \\ \theta^1 \\ \vdots \\ \theta^J \end{bmatrix}
\tag{2.71}
$$

In typical DPD systems, the number of measured samples is much higher than the number of coefficients to be estimated. This results in an overdetermined system of equations to be solved. Least squares (LS) based approaches are a widely used technique for model and DPD identification tasks. The least squares estimator finds coefficients such that the sum of squared errors between the chosen model and the observation data is minimized. In matrix-vector notation, i.e. for a vector of coefficients as in (2.69), the cost function J is given by

$$
J = (\mathbf{y} - \mathbf{H}\,\boldsymbol{\theta})^H \, (\mathbf{y} - \mathbf{H}\,\boldsymbol{\theta}).
\tag{2.72}
$$

Using the Wirtinger calculus [79, 80] the coefficients $\boldsymbol{\theta}$ can be estimated by

$$
\hat{\boldsymbol{\theta}} = \left(\mathbf{H}^H\,\mathbf{H}\right)^{-1} \mathbf{H}^H \mathbf{y}.
\tag{2.73}
$$

Instead of the batch approach (2.73), the least squares solution can be calculated on a sample by sample basis with the recursive LS algorithm, preventing the computation of a matrix inverse $\left(\mathbf{H}^H\,\mathbf{H}\right)^{-1}$ [81–83].

Another adaptive estimation approach is the least mean squares (LMS) algorithm [84, 85], which is based on the stochastic gradient technique. Again, assuming a linear model

$$
y[k] = \mathbf{h}^H[k]\,\boldsymbol{\theta}
\tag{2.74}
$$

the complex LMS algorithm is given by

$$
\boldsymbol{\theta}[k+1] = \boldsymbol{\theta}[k] - \mu\,e^*[k]\,\mathbf{h}[k],
\tag{2.75}
$$

where $e[k] = y[k] - \mathbf{h}^H[k]\boldsymbol{\theta}[k]$ is the instantaneous error for the kth sample. By using the instantaneous error, neither the autocorrelation nor the cross-correlation

matrix are required for (2.75) as one e. g. would have to know when calculating the Wiener filter solution [85]. The LMS update algorithm (2.75) is straight forward to implement and offers a valuable tradeoff between complexity and convergence. However, because of the underlying stochastic approach, convergence time may suffer due to the high spreading of the eigenvalues of the instantaneous correlation matrix $\mathbf{R}_{hh}[k] = \mathbf{h}[k]\,\mathbf{h}^H[k]$.

Adaptive model fitting and learning techniques for DPD models are typically classified into direct and indirect learning approaches, as depicted in Figures 2.13a and 2.13b, respectively. The difference between these two approaches is the definition of the error signal and the filling of the nonlinear functionals in the matrix $\mathbf{H}$ with either the input signal or the output signal of the RF-PA, respectively. An additional method, the so-called forward identification is shown in Figure 2.13c. While direct and indirect learning are used for DPD systems, forward identification typically serves for RF-PA identification purposes due to the (complicated) required inversion of the identified PA model $\{F_{\mathrm{PA}}\,\{\cdot\}\}^{-1}$, which is needed to calculate the coefficients of the predistorter.

The coefficient estimation requires that the raw output data of the RF-PA is attenuated and synchronized to the input signal, including delay correction Δt and phase correction $\Delta\varphi$. Delay and phase correction can also be applied on the input signal, as indicated in Figure 2.13. The magnitude scaling is usually chosen to be equivalent to the ideal (RMS) gain g_{RMS} of the RF-PA ensuring that the output of the whole system with DPD converges to the same output RMS as without DPD. However, there are different gain adjustment options such as the maximum gain or even variable gains, which depend on the current output power of the RF-PA [86]. Time delay and phase rotation are estimated based on their complex cross-correlation [7].

The following discussion uses linear models such as in (2.69), where the block matrix $\mathbf{H}$ consist of nonlinear basis functions such as the memory polynomial. Furthermore, estimation is reduced to the LS algorithm.

Adaptive predistortion requires to iteratively update the DPD coefficients. In integrated DPD systems the number of samples is limited. Thus several iterations are typically performed to get some averaging of the noisy output samples $y[k]$ of the RF-PA. At each iteration the DPD coefficients are updated based on an (estimated) coefficient error vector $\Delta\boldsymbol{\theta}$ [10], i. e.

$$\boldsymbol{\theta}_{i+1} = \boldsymbol{\theta}_i - \mu\,\Delta\boldsymbol{\theta}, \tag{2.76}$$

where i is the iteration index, and μ is a constant used to control the speed of convergence and the stability of the iteration process.

In the direct learning approach, as shown in Figure 2.13a, the error is the difference between the (scaled) output of the RF-PA and the (synchronized) input signal, i. e.
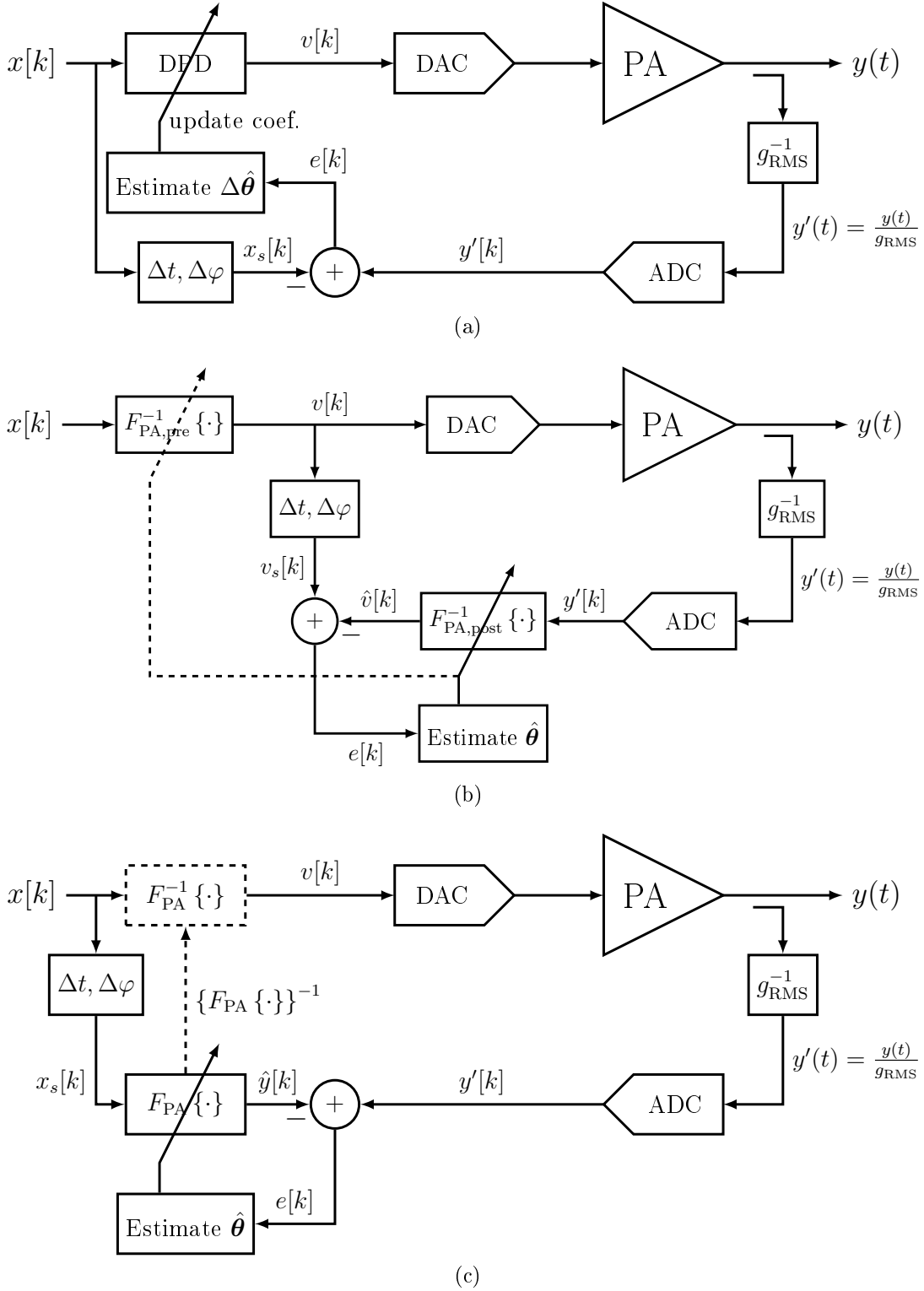
$$\mathbf{e} = \mathbf{y}' - \mathbf{x}_s, \tag{2.77}$$

(a)

(b)

(c)

Figure 2.13: Block diagram of the (a) direct learning, (b) indirect learning, and (c) forward identification method.

This error signal is related to the error in the DPD coefficients $\Delta\boldsymbol{\theta}$ [7] as

$$\mathbf{e} = \mathbf{H}_x\,\Delta\boldsymbol{\theta} \qquad (2.78\text{a})$$

$$\mathbf{y}' - \mathbf{x}_s = \mathbf{H}_x \cdot \Delta\boldsymbol{\theta} \qquad (2.78\text{b})$$

where $\mathbf{H}_x$ is the nonlinear block model matrix filled with the input signal samples. The coefficient errors $\Delta\hat{\boldsymbol{\theta}}$ are estimated by minimizing the difference between the error and the predistortion update [10]:

$$J = \min \sum_k \left| e[k] - \sum_{j=1}^{J} \Delta\theta_j\, h_j\left(x_s[k]\right) \right|^2, \qquad (2.79)$$

where $h_j\left(x[k]\right)$ describes the nonlinear basis function for $x[k]$. The coefficient error vector can thus be estimated by

$$\Delta\hat{\boldsymbol{\theta}} = \left(\mathbf{H}_x^H\,\mathbf{H}_x\right)^{-1}\mathbf{H}_x^H \cdot \left(\mathbf{y}' - \mathbf{x}_s\right), \qquad (2.80)$$

and the updated DPD coefficient are

$$\boldsymbol{\theta}_{i+1} = \boldsymbol{\theta}_i - \mu\,\Delta\hat{\boldsymbol{\theta}}. \qquad (2.81)$$

The DPD works in closed-loop, similar to a controller in digital control theory concepts. Henceforth, also other estimation approaches such as the LMS algorithm can be used. Alternatively, an additional RF-PA model can be used as input to the coefficient estimation process [10].

In contrast to the direct learning method, the indirect learning operates as an open-loop system. A special case of the indirect learning, where the DPD coefficients are directly estimated is shown in Figure 2.13b. This concept estimates an inverse model of the RF-PA $F_{\mathrm{PA}}^{-1}\left\{\cdot\right\}$ by minimizing the error between the input signal and the postdistorted output signal of the RF-PA, i.e.

$$\mathbf{e} = \mathbf{v}_s - \mathbf{H}_{y'}\,\boldsymbol{\theta}, \qquad (2.82)$$

where $H_{y'}$ is the nonlinear model matrix filled with the (scaled) output of the RF-PA, and $\mathbf{v}_s$ contains the time and phase synchronized input samples of the RF-PA after the predistorter. This approach is referred to as postdistortion as the output of the RF-PA passes through the nonlinear model or as inverse identification as the postdistorter models the "inverse" of the RF-PA nonlinearity. Minimizing the error (2.82) in an LS manner results in the cost function

$$J = \min \sum_k \left| v_s[k] - \sum_{j=0}^{J} \left[\theta_j\, y'^j[k]\right] \right|^2, \qquad (2.83)$$

and the postdistorter coefficients are given by

$$\hat{\boldsymbol{\theta}} = \left(\mathbf{H}_{y'}^H\,\mathbf{H}_{y'}\right)^{-1}\mathbf{H}_{y'}^H \cdot \mathbf{v}_s. \qquad (2.84)$$

The estimated coefficients $\hat{\boldsymbol{\theta}}$ are directly used in the predistorter as indicated in Figure 2.13b. The first indirect learning for RF-PA linearization was mentioned in [87], and first applied (published) to solid-state RF-PA's by Ding et al. [23, 24] using memory polynomial models. The estimator in (2.84) is designed to find the best postdistorter coefficients. However, these coefficients are in general not the optimum coefficients for the predistorter [7] due to the nonlinear nature of the overall system, which is a weakness of the indirect learning approach. Nevertheless, equations (2.82) and (2.84) describe the estimation approach for a one-time calibration, i.e. the coefficients are not updated from previously performed estimation approaches. To extend the concept to an adaptive (iterative) approach the error expression for a given estimation block uses the previously calculated coefficients [10]

$$\mathbf{e}_{\Delta} = \mathbf{H}_{y'_{i+1}}\,\boldsymbol{\theta}_i - \mathbf{v}_{s_{i+1}}, \tag{2.85}$$

where $\mathbf{H}_{y'_{i+1}}$ and $\mathbf{v}_{s_{i+1}}$ are the model matrix and the input signal vector at the $(i+1)$-th iteration, respectively. $\boldsymbol{\theta}_i$ are the predistorter coefficients used from the previous iteration to generate $\mathbf{v}_{s_{i+1}}$. The corresponding cost function is

$$J_{\Delta} = \min \sum_k \left| e[k] - \sum_{j=1}^{J} \Delta\theta_j\, h_j\left(y'[k]\right) \right|^2, \tag{2.86}$$

where $h_j\left(y'[k]\right)$ describes the nonlinear basis function for $y'[k]$. The resulting error vector for the coefficient update $\Delta\hat{\boldsymbol{\theta}}$ can be estimated by

$$-\Delta\hat{\boldsymbol{\theta}} = \boldsymbol{\theta}_i - \boldsymbol{\theta}_{i+1} = \left(\mathbf{H}_{y'_{i+1}}^H\, \mathbf{H}_{y'_{i+1}}\right)^{-1} \mathbf{H}_{y'_{i+1}}^H\, \mathbf{e}_{\Delta}. \tag{2.87}$$

Rearranging (2.87) shows that the coefficient error vector can be described by $\mathbf{e}_{\Delta} = -\mathbf{H}_{y'_{i+1}}\Delta\boldsymbol{\theta}$, and the resulting update equation for the next DPD coefficients is then given by

$$\boldsymbol{\theta}_{i+1} = \boldsymbol{\theta}_i - \mu\,\Delta\hat{\boldsymbol{\theta}}, \tag{2.88}$$

which is similar as for the direct learning approach. However, the underlying considerations and hence calculations of $\Delta\hat{\boldsymbol{\theta}}$ are different.

The forward identification concept, as shown in Figure 2.13c, tries to minimize the error between an RF-PA model and the actual output of the RF-PA, i.e.

$$\mathbf{e} = \mathbf{y}' - \mathbf{H}_x\,\boldsymbol{\theta}. \tag{2.89}$$

The concept is similar to typically used system identification approaches in signal processing. Forward identification is also used in an open-loop configuration and can thus also be seen as a special case for the indirect learning method. For the coefficient estimation the DPD is not active as indicated by the dashed line in Figure 2.13c and hence $v[k] = x[k]$. The resulting least squares cost function is

$$J = \min \sum_k \left| y'[k] - \sum_{j=1}^{J} \theta_j\, h_n\left(x_s[k]\right) \right|^2. \tag{2.90}$$

The coefficients can then be estimated by

$$\hat{\boldsymbol{\theta}} = \left(\mathbf{H}_x^H \, \mathbf{H}_x\right)^{-1} \mathbf{H}_x^H \cdot \mathbf{y}'. \tag{2.91}$$

For the predistorter, the nonlinear model must then be "inverted", indicated in Figure 2.13c by $\{F_{\mathrm{PA}}\{\cdot\}\}^{-1}$ from the RF-PA model to the DPD. Typically this requires complex mathematical manipulations. Furthermore, not all nonlinear models can be inverted. Thus this method is hardly used for directly calculating the predistorter coefficients but finds its use for RF-PA modeling and characterization. However, Wang et. al [88] showed that the forward identification can be used in a hybrid indirect learning approach, where the estimated RF-PA model is used as input to a parallel working postdistorter, which inherently calculates the "inverse" nonlinearity for the predistorter.

3 Modeling of Capacitive RF-DACs

Modeling of circuits for system-level simulations is a major task during the design phase of integrated circuits. The design and specification of system blocks require accurate and applicable abstract models. While circuit-level simulators focus on the verification of a specific block, system-level simulations target specifying and validating complete systems, e.g. a complete transmitter for wireless communications.

Circuit simulators achieve the best accuracy, as sophisticated physical device models accurately model integrated circuit components. However, these kinds of simulators are practically infeasible for system-level simulation setups as with the accuracy, also the required simulation time increases. On the other hand, behavioral models, described in Section 2.2.2, are a commonly used approach to model nonlinear systems, where very short simulation run times can be achieved, providing a highly useful tool for system-level simulations. However, the behavior of the model does no longer correspond to the physics of the underlying circuit. Slight changes of the circuit structure or its parameters could cause significant changes in the behavior, requiring re-estimation of the model parameters or even requiring a different mathematical model. Furthermore, a black box approach prohibits the analysis and simulation of dedicated circuit-related error sources such as clock jitter, supply noise, or component mismatch of distinct parts of the circuit.

This chapter presents a modeling concept for the capacitive RF-DAC, which keeps the relation to the underlying circuit and additionally provides short simulation run times. The following models are based on the switched state-space methodology, which is often used to model hybrid systems [89–91]. The technique results in short simulation run times and provides the possibility to simulate distinct nonideal behavior of the circuitry such as cell mismatch, supply voltage variation, and clock jitter. However, the derived models are not equivalent baseband models, but inherently contain the mixing operation of the capacitive RF-DAC. The output, as well as system states can therefore directly be evaluated in the RF domain.

This chapter is organized as follows. First, the methodology of switched state-space models is briefly explained. Next, the technique of linear switched state-space models is used to derive a model for the polar RF-DAC. Furthermore, the concept is also applied to the quadrature RF-DAC architecture. To further improve accuracy, the linear approach is extended to a nonlinear model to cover AM-PM

characteristics, which are caused by the dynamic behavior of the switching transistors. Finally, the chapter concludes showing the possibility to model nonideal circuit behavior such as jitter, cell mismatch, and supply noise.

3.1 Switched State-Space Models

In system and control theory, state-space models are a well-known method to describe electrical circuits and systems. In recent years, the switched state-space modeling approach was extensively used to analyze and simulate switched systems and circuits [92–95]. These so-called hybrid systems are composed of a set of subsystems and a high-level switching law, which determines the active subsystem. In state-space representation, a dynamic system is described by first order differential equations [89]

$$\frac{d}{dt}\mathbf{z}(t) = f_{\sigma(t)}\left[\mathbf{z}(t), \mathbf{u}(t)\right], \tag{3.1a}$$

$$\mathbf{y}(t) = g_{\sigma(t)}\left[\mathbf{z}(t), \mathbf{u}(t)\right]. \tag{3.1b}$$

The state vector $\mathbf{z} \in \mathbb{R}^{\alpha}$, the output vector $\mathbf{y} \in \mathbb{R}^{\gamma}$, and the control (input) vector $\mathbf{u} \in \mathbb{R}^{\beta}$ in (3.1a) and (3.1b) take on values from a continuous space. The functions $f_m(\cdot)$ and $g_m(\cdot)$ describe the dynamic behavior of the m-th subsystem, where $m = \sigma(t)$ at time t. The switching signal $\sigma(t)$ is a discrete valued and piecewise constant signal, i.e. $\sigma(t) \in \mathcal{D} = \{1, 2, \ldots, D\}$. The discrete state of $\sigma(t)$ may depend on multiple internal or external input signals,

$$\sigma(t^{+}) = \psi\left[t, \sigma(t), \mathbf{z}(t), \mathbf{y}(t), \mathbf{p}(t)\right], \tag{3.2}$$

where $\sigma(t^{+}) = \lim_{s \to t^{+}} \sigma(s)$ [90]. The next state of the switching signal $\sigma(t^{+})$ may depend on the time t, former values of the switching signal $\sigma(t)$, the system states $\mathbf{z}(t)$, the system outputs $\mathbf{y}(t)$, or external signals $\mathbf{p}(t)$. The switching signal can be interpreted as a multiplexer that selects the active subsystem at time instant t. Fig. 3.1 illustrates the structure of such a switched system.

The overall system consists of d subsystems, where only one subsystem is active at any time instant, depending on the state of $\sigma(t)$. It follows that the dynamic behavior of the overall system is determined by the switching signal $\sigma(t)$ and the internal dynamics of each subsystem $f_m(\cdot)$ and $g_m(\cdot)$, where $m = \sigma(t)$.

A special class of these hybrid systems are so called switched linear systems, where all subsystems are restricted to be linear and time-invariant (LTI). In hybrid system theory, one way to model such kind of systems is the switched linear state-space model (LSSM). The mathematical form of a continuous time switched LSSM is given by

$$\frac{d}{dt}\mathbf{z}(t) = \mathbf{A}_{\sigma(t)}\,\mathbf{z}(t) + \mathbf{B}_{\sigma(t)}\,\mathbf{u}(t), \tag{3.3a}$$

$$\mathbf{y}(t) = \mathbf{E}_{\sigma(t)}\,\mathbf{z}(t) + \mathbf{F}_{\sigma(t)}\,\mathbf{u}(t), \tag{3.3b}$$
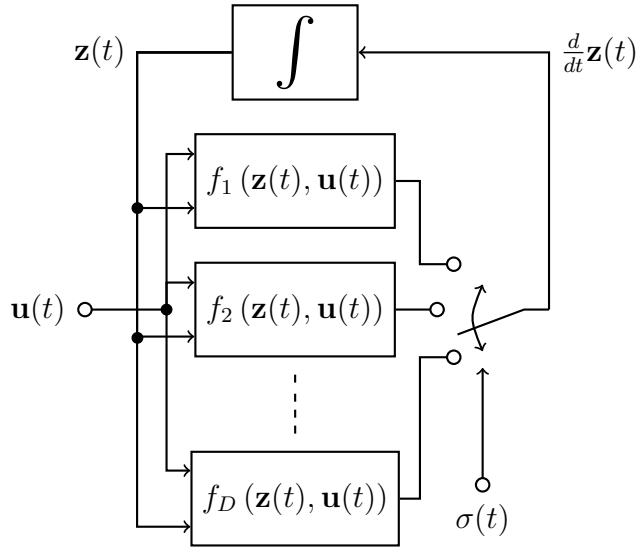
Figure 3.1: Structure of a hybrid system, where a dedicated switch selects the active subsystem, depending on the switching signal $\sigma(t)$.

where $\mathbf{z}(t)$ is the state vector and $\mathbf{u}(t)$ represents the independent inputs of the system in vector notation. The matrices $\{\mathbf{A}_m, \mathbf{B}_m, \mathbf{E}_m, \mathbf{F}_m\}$ define the so-called local dynamics and the output $\mathbf{y}(t)$ of the m-th subsystem, respectively. To simplify notation and to avoid too long indices $\{\mathbf{A}, \mathbf{B}, \mathbf{E}, \mathbf{F}\}_m$ is used instead of $\{\mathbf{A}_m, \mathbf{B}_m, \mathbf{E}_m, \mathbf{F}_m\}$ further on. As above $\sigma(t)$ is the switching signal and determines the active subsystem at time t.

Keeping the same state variables for all subsystems is a necessary requirement to model switching circuits such as the capacitive RF-DAC with switched state-space models. This holds for a continuous-time as well as for discrete-time systems. Hence, the elements of the state vector $\mathbf{z}(t)$ must represent the same system states for each subsystem. The state vector $\mathbf{z}(t)$ of the current system $\{\mathbf{A}, \mathbf{B}, \mathbf{E}, \mathbf{F}\}_{\sigma(t_i)}$ is then used as set of initial conditions for the next system configuration $\{\mathbf{A}, \mathbf{B}, \mathbf{E}, \mathbf{F}\}_{\sigma(t_{i+1})}$ at a switching transition, i.e. when $\sigma(t_i) \neq \sigma(t_{i+1})$ for $t_i < t_{i+1}$. Furthermore, the switching transitions from one discrete state to another one are assumed to be instantaneous.

The implementation on digital computers and numerical simulators requires a discrete time representation of (3.3a) and (3.3b). There are well established methods to discretize the continuous time models [96]. The general form of a discrete time switched LSSM is given by

$$\mathbf{z}[k+1] = \mathbf{A}_{d_{\sigma[k]}} \mathbf{z}[k] + \mathbf{B}_{d_{\sigma[k]}} \mathbf{u}[k], \tag{3.4a}$$

$$\mathbf{y}[k] = \mathbf{E}_{d_{\sigma[k]}} \mathbf{z}[k] + \mathbf{F}_{d_{\sigma[k]}} \mathbf{u}[k], \tag{3.4b}$$

with k representing the discrete time instances $k\,T_s$. The corresponding discrete state-space matrices $\{\mathbf{A}_d, \mathbf{B}_d, \mathbf{E}_d, \mathbf{F}_d\}_{\sigma[k]}$, are approximated by the zero-order hold (ZOH) method, where the input $\mathbf{u}(t)$ is assumed to be constant over one simulation

time step T_s [97], which leads to

$$\mathbf{A}_{d_m} = e^{\mathbf{A}_m \cdot T_s}, \tag{3.5a}$$

$$\mathbf{B}_{d_m} = \mathbf{A}_m \left(\mathbf{A}_{d_m} - \mathbf{I}\right)^{-1} \mathbf{B}, \tag{3.5b}$$

$$\mathbf{E}_{d_m} = \mathbf{E}_m, \tag{3.5c}$$

$$\mathbf{F}_{d_m} = \mathbf{F}_m. \tag{3.5d}$$

The ZOH method ensures that the same state variables are used for all subsystems after discretization. This can be intuitively seen as matrices $\mathbf{E}_{d_m}$ and $\mathbf{F}_{d_m}$ are equivalent to the continuous time ones. Thus $\mathbf{z}[k]$ and $\mathbf{y}[k]$ must represent the same system states. The output $\mathbf{y}[k]$ is a good approximation of $\mathbf{y}(t)$ as in (3.3b) at discrete time instances $k\,T_s$ if the input $\mathbf{u}[k]$ is slowly varying between two consecutive time steps T_s. Thus the simulation step size T_s must be chosen adequately. Other discretization methods such as the Tustin approximation may yield better results at lower sampling frequencies f_s but change the representation of the state vector for each circuit configuration [96], and can thus not be used for switched state-space models.

3.2 Switched Linear State-Space Models

3.2.1 Switched Linear State-Space Model for Polar Capacitive RF-DACs

A simplified schematic of a polar capacitive RF-DAC is shown in Fig. 3.2. With the LO one electrode of the active cell capacitors toggles between V_{DD} and V_{SS}. On top of that, the number of active cells $n(t)$ is determined by the input signal $\tilde{x}(t)$, which also dynamically changes the circuit configuration over time. Hence, the circuit can't be modeled by a time-invariant model for transient simulations. Furthermore, due to the dependency on the input code, typical small-signal simulation techniques can't be used to fully analyze and simulate the behavior. Consequently, a time-variant model is required to cover the LO switching effect and the amplitude modulation by the input code.

Typical capacitive RF-DAC architectures consist of thousands of unitary and a few binary-weighted cells [3,4]. Hence, one problem for the state-space approach is the vast number of potential system states, in case one state variable is introduced for each capacitor. Then the state vector would consist of $(N_{\text{thermo}} + N_{\text{binary}} + 1)$ states, where $+1$ is due to the inductor in the (simplified) matching network. Henceforth, this would lead to a significant large number of required numerical calculations, counteracting the goal of a fast transient model.

However, when considering the structure of the capacitive RF-DAC as shown in Fig. 3.2, all n active cells and all $(N - n)$ static cells are connected in parallel. Assuming that all active/static cells are switched with the LO simultaneously, the parallel structure can be simplified to two equivalent cells as shown in Fig. 3.3.
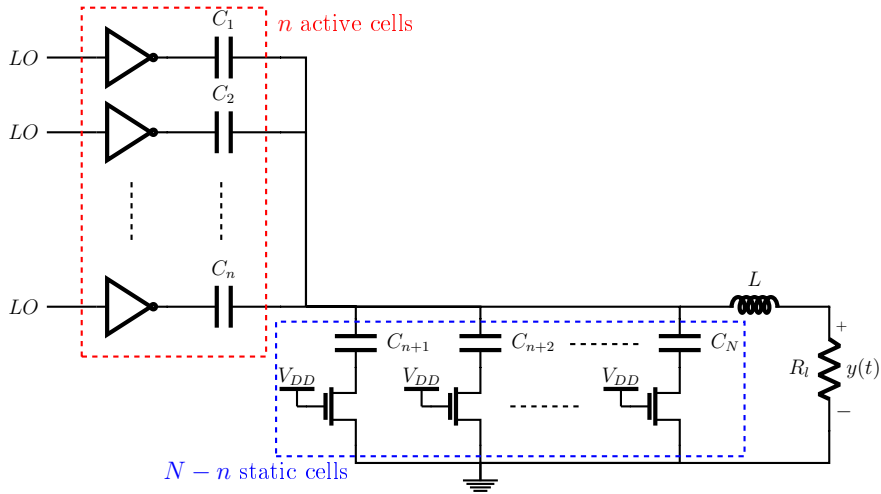
Figure 3.2: Simplified schematic of a capacitive RF-DAC with n active and $N - n$ static cells, respectively.

With that, the required states are reduced to three, heavily relaxing the required computation effort.
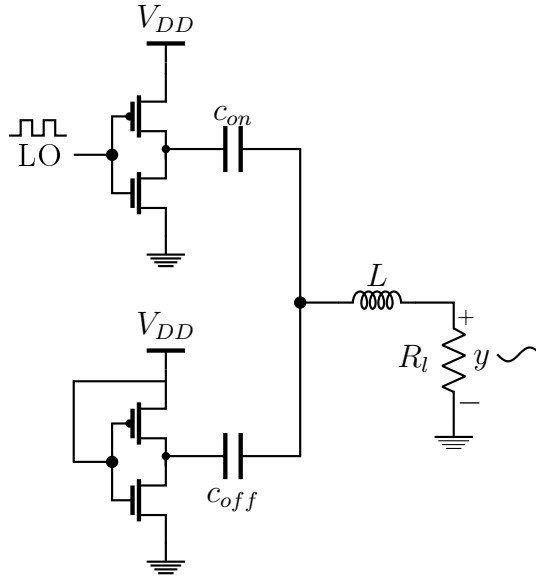

Figure 3.3: Capacitive RF-DAC circuit with equivalent active/static cells.

One of the main contributors to the nonlinear behavior of the capacitive RF-DAC, especially AM-PM distortion, is the parasitic on-resistance of the PMOS and NMOS transistors [30]. In the model the unit cell inverters are replaced by an equivalent circuit based on lumped components, which allows to use switched LSSM and accounts for the dominating parasitic effects. The inverter's equivalent circuit, as shown in Figure 3.4, is a parallel combination of channel losses described by a resistor $r_{on,n}$ $(r_{on,p})$ and a parasitic capacitance to the substrate c_p, which is
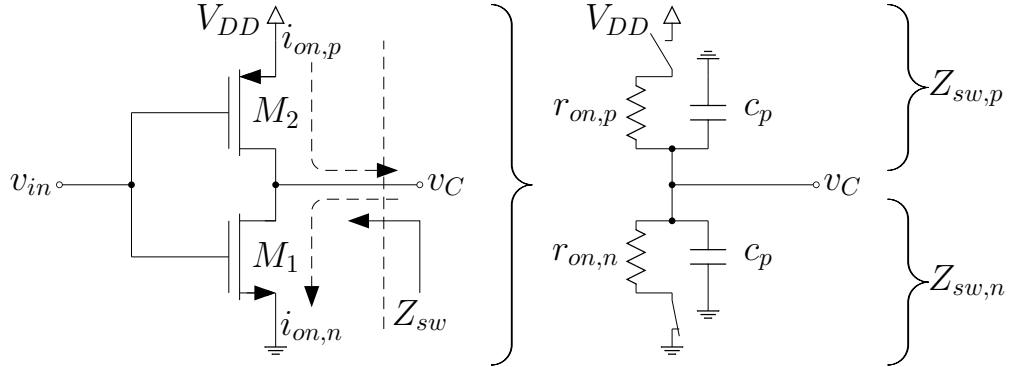
Figure 3.4: CMOS inverter and equivalent circuit for the active devices. The output v_C toggles between ground and supply.

assumed equal for both NMOS and PMOS devices. Additionally, Figure 3.4 also sketches the charging and discharging currents flowing through the transistors. The accumulated switch parasitic drain capacitance, however, has only little impact on the circuit performance since it scales with technology. Hence, in sub-micron implementations, it can be considered as a second-order effect and is neglected in the following. Thus the NMOS/PMOS transistors are modeled by semi-ideal switches, where the off-state is assumed to be ideal (infinite on-resistance), and the on-resistance is represented by the parasitic ohmic losses of the channel. Similar approaches are also used for analyzing and designing DC-DC switching convert-ers [91]. Typically, the channel width of PMOS transistors is roughly twice the size of their NMOS counterparts to overcome the reduced positive charge carrier mobility. The purpose is to ensure equal on-resistances for the charging networks.

In the proposed model the equivalent on-resistance is determined by static DC analysis of the actual implemented cell transistors with circuit simulators such as Spice or SpectreRF$^{\circledR}$. A constant small V_{DS} voltage, keeping the transistor in the triode region, is connected to the drain-source connections and the current through the device is measured. The on-resistance can then be calculated by the constant voltage drop V_{DS} divided by the measured drain (source) current I_{DS}.

With the above mentioned assumptions, the number of states can be reduced and the nonlinear devices are replaced by lumped components. Henceforth, the equivalent active and inactive cell from Figure 3.3 reduces to a single impedance composed of the respective transistor on-resistance $r_{on_{p/n}}$ in series with the cell capacitor $c_{on/off}$. The particular on-resistances are assumed to be constant over the whole switching period and are thus evaluated for $V_{GS} = V_{DD}$, and $V_{GS} = V_{SS}$ for the NMOS and PMOS, respectively.

Nevertheless, with the changing input signal, the active and inactive cell capac-itor and equivalent on-resistances still change dynamically with the input code. Thus, as a next step, the input signal is assumed to be constant, i. e. $n(t) = n \, \forall t \in \mathbb{R}^+$. The circuit structure then only changes with the LO signal, which is used as

the switching signal $\sigma(t) \in \mathcal{D}_{\text{LO}} = \{0, 1\}$, i. e.

$$\sigma(t) = \begin{cases} 0 & \text{when LO} = V_{SS} \\ 1 & \text{when LO} = V_{DD} \end{cases} \tag{3.6}$$

The resulting lumped models for the two possible LO states can then be represented by two circuits shown in Figure 3.5, where

$$c_{on} = C_1 + C_2 + \cdots + C_n, \tag{3.7a}$$

$$c_{off} = C_{n+1} + C_{n+2} + \cdots + C_N, \tag{3.7b}$$

$$r_{on} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n}}, \text{ with } R_i = r_{on_{p/n}}, \tag{3.7c}$$

$$r_{off} = \frac{1}{\frac{1}{R_{n+1}} + \frac{1}{R_{n+2}} + \cdots + \frac{1}{R_N}}, \text{ with } R_j = r_{on_n}, \tag{3.7d}$$

with $\sigma(t) = 0 \rightarrow R_i = r_{on_p}$, and $\sigma(t) = 1 \rightarrow R_i = r_{on_n}$. The on-resistance of the static cells depend only on the NMOS parasitics, i. e. $R_j = r_{on_n}$.

The state vector, for both subsystems, is defined as

$$\mathbf{z}(t) = \begin{bmatrix} v_{c_{on}}(t) \ v_{c_{off}}(t) \ i_L(t) \end{bmatrix}^T. \tag{3.8}$$

Each subsystem, sketched in Figure 3.5, can thus be described by a linear state-space model. With the switching signal $\sigma(t)$ the state-space matrices for each circuit configuration can be combined to form a switched linear state-space model as in (3.3a) and (3.3b). The input is the supply voltage of the inverter circuit, $\mathbf{u}(t) = V_{DD}$. The output is specified as the voltage drop across the load resistor, $y(t) = i_L(t) R_l$.

Nevertheless, in addition to the LO switching, also the modulation introduced by the input signal and thus the changing structure related to the number of active cells $\tilde{x}(t) \rightarrow n(t)$ must still be considered. With a finite number of cells, $n(t)$ is also discrete valued, i. e. $n(t) \in \mathcal{N}_{polar} = \{1, \ldots, N\}$. Thus, the number of active cells, and hence the circuit configuration change at discrete time steps and to a finite number of subsystems. It follows that the active subsystem of the polar capacitive RF-DAC at time instant t depends on the LO switching $\sigma(t)$ and the number of active switching cells $n(t)$. The overall switched system can thus be mathematically expressed using the switched LSSM

$$\frac{d}{dt}\mathbf{z}(t) = \mathbf{A}_{\sigma(t),n(t)} \, \mathbf{z}(t) + \mathbf{B}_{\sigma(t),n(t)} \, V_{DD}, \tag{3.9a}$$

$$y(t) = \mathbf{E} \, \mathbf{z}(t). \tag{3.9b}$$

The continuous time state-space matrices for the different LO states are given in the following. The resulting state-space matrices for switching state $m = 0$ are:
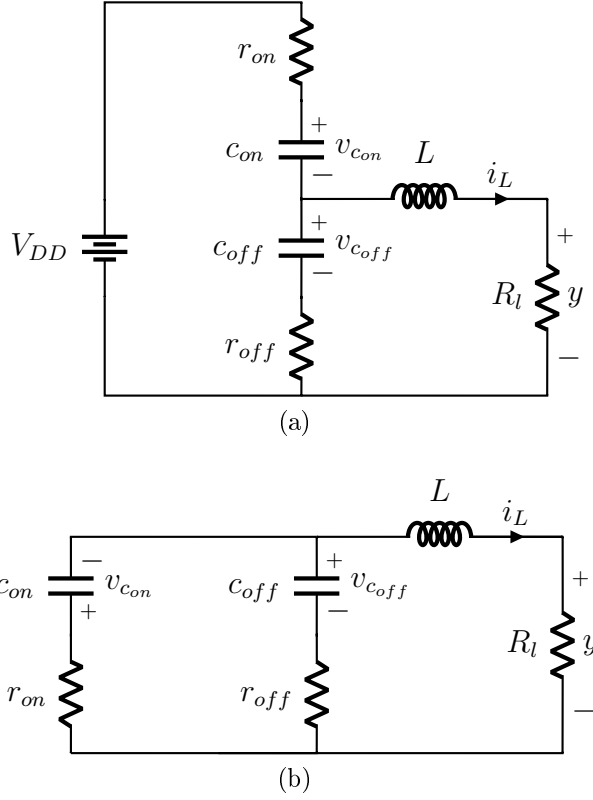
Figure 3.5: Equivalent circuits of the polar capacitive RF-DAC for both LO states. (a) $\sigma(t) = 0$, (b) $\sigma(t) = 1$.

$$\mathbf{K}_{0,n} = \begin{bmatrix} c_{on} & 0 & 0 \\ 0 & c_{off} & 0 \\ 0 & 0 & L \end{bmatrix} \tag{3.10a}$$

$$\mathbf{A}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & 1 - \frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{r_{off}}{r_{on}+r_{off}} & 1 - \frac{r_{off}}{r_{on}+r_{off}} & -\left(R_l + \frac{r_{on} \, r_{off}}{r_{on}+r_{off}}\right) \end{bmatrix} \tag{3.10b}$$

$$\mathbf{B}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} \frac{1}{r_{on}+r_{off}} \\ 1 \\ \frac{r_{off}}{r_{on}+r_{off}} \end{bmatrix} \tag{3.10c}$$

$$\mathbf{E}_{0,n} = \begin{bmatrix} 0 & 0 & R_l \end{bmatrix} \tag{3.10d}$$

$$\mathbf{F}_{0,n} = 0 \tag{3.10e}$$

where $r_{\mathrm{on}} = f\left(r_{\mathrm{on}_p}\right)$. One can see that the output matrix $\mathbf{E}_{m,n}$ and the feed forward matrix $\mathbf{F}_{m,n}$ are independent of the switching states m and n. Thus, only the dynamic and the control matrix change with the circuit configurations. Hence, indices m and n for $\mathbf{E}_{m,n}$ and $\mathbf{F}_{m,n}$ will be skipped in the following. Matrix $\mathbf{K}_{m,n}$

is independent of the switching state m and only depends on the current number of active cells n. Therefore, m in $\mathbf{K}_{m,n}$ is also skipped from here on.

For the other LO switching state $m = 1$, it can be shown that the dynamic matrix $\mathbf{A}_{m,n}$ possesses the same entries as for $m = 0$ in (3.10b). However, the on-resistance changes and depends on the NMOS on-resistance $r_{\mathrm{on}} = f(r_{\mathrm{on}_n})$. Hence, the state-space matrices for $m = 1$ are given by:

$$\mathbf{A}_{1,n} = \mathbf{A}_{0,n}, \text{with } r_{\mathrm{on}} = f(r_{\mathrm{on}_n}) \tag{3.11a}$$

$$\mathbf{B}_{1,n} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.11b}$$

$$\mathbf{E}_{1,n} = \mathbf{E}_{0,n} = \mathbf{E} \tag{3.11c}$$

$$\mathbf{F}_{1,n} = \mathbf{F}_{0,n} = \mathbf{F} = 0 \tag{3.11d}$$

Assuming that the on-resistances of the transistors are the same, i.e. $r_{on_p} = r_{on_n}$, the dynamic matrix of (3.10b) is equivalent to (3.11a) and hence only the control matrix $\mathbf{B}_{m,n}$ changes with the LO signal.

As described above, polar architectures modulate the phase on the LO signal dependent on the input signal's phase information. Hence, the simulation step size must be set accordingly to the required resolution of the modulated rise/fall times of the phase changes of the LO.

3.2.2 Switched Linear State-Space Model for Quadrature Capacitive RF-DACs

This section extends the modeling concept of the polar capacitive RF-DAC architecture to the quadrature design. As described in Chapter 2.1, the capacitive RF-DAC can also be designed to process quadrature data signals, where the DFE passes two input code signal streams. The resulting number of active cells is proportional to the magnitudes of the real and the imaginary components of the complex valued data stream $\tilde{x}(t) = x_I(t) + j\,x_Q(t)$, i.e. $n_I(t) \propto |x_I(t)|$ and $n_Q(t) \propto |x_Q(t)|$. In the classical design, the capacitor cell array is separated into in-phase and quadrature signal related cells, respectively. Hence, each component can trigger up to $\frac{N}{2}$ cells. The active switching cells are driven by two 90° phase-shifted LO signals, respectively. Compared to the polar architecture, the phases of the I and Q LO signals are not modulated.

Negative input codes of $x_I(t)$ and $x_Q(t)$ are realized by shifting the phase of the respective LO by 180°. This phase shift is a critical part of the quadrature capacitive RF-DAC design. Imperfect timing leads to distortion and increased noise floor in the output signal spectrum [49].

The input codes are part of the discrete set $(n_I(t), n_Q(t)) \in \{1, \ldots, \frac{N}{2}\} \times \{1, \ldots, \frac{N}{2}\}$ The total number of active and inactive cells at time instant t is thus

given by

$$n_{on} = n_I(t) + n_Q(t), \tag{3.12a}$$

$$n_{off} = N - n_I(t) - n_Q(t). \tag{3.12b}$$

The derivation of the switched LSSM of the quadrature capacitive RF-DAC is performed by following the same steps as in the polar case. First, the input code is assumed to be constant, i.e. $n_I(t) = n_I$ and $n_Q(t) = n_Q$. Further, $\sigma_I(t) \in \mathcal{D}_{\text{LO}}$ and $\sigma_Q(t) \in \mathcal{D}_{\text{LO}}$ represent the in-phase and the quadrature LO signal, similarly defined as in (3.6). The transistors are modeled by a semi-ideal switch with infinite high off-resistance and an equivalent on-resistance. The on-resistance of the transistors depends on the respective switching signals $\sigma_I(t)$ and $\sigma_Q(t)$ with $r_{on,p}$ for $\sigma_j(t) = 0$ and $r_{on,n}$ for $\sigma_j(t) = 1$ for $j \in (I, Q)$. Equivalent capacitor and resistor values for each subsystem are determined by the relations in (3.7a) - (3.7d), but depending on $n_I(t)$ and $n_Q(t)$, respectively.

All circuit configurations for a fixed number of switching cells n are shown in Fig. 3.6. Fig. 3.6b shows the circuit configuration for $\sigma_I(t) = 0, \sigma_Q(t) = 1$ but can be used interchangeably for the state $\sigma_I(t) = 0$, $\sigma_Q(t) = 1$ by changing indices $_I$ and $_Q$. The elements of the state vector are again defined as the voltages over the capacitors and the current through the inductor:

$$\mathbf{z}(t) = \begin{bmatrix} v_{c_{I_{on}}}(t) & v_{c_{Q_{on}}}(t) & v_{c_{off}}(t) & i_L(t) \end{bmatrix}^T. \tag{3.13}$$

Both, I and Q cells are connected to the same power supply and thus $\mathbf{u}(t) = V_{DD}$. The output is, as for the polar capacitive RF-DAC, the voltage across the load resistor, i.e. $y(t) = i_L R_l$.

Nevertheless, if the input code is no longer restricted to be constant, new subsystems are introduced, which are related to $n_I(t)$ and $n_Q(t)$. Applying again the same principle as for the polar architecture, the number of active switching cells $n_I(t)$ and $n_Q(t)$ are treated as additional switching signals Although the switching state of the state-space matrices depends on four signals, i.e. $\sigma_I(t), \sigma_Q(t), n_I(t), n_Q(t)$, the number of possible subsystems is only doubled compared to the polar capacitive RF-DAC as the number of total cells N is assumed to be the same. Finally, the overall model of the quadrature capacitive RF-DAC can be mathematically described by the switched LSSM:

$$\frac{d}{dt}\mathbf{z}(t) = \mathbf{A}_{\sigma_I(t),\sigma_Q(t),n_I(t),n_Q(t)} \, \mathbf{z}(t) + \mathbf{B}_{\sigma_I(t),\sigma_Q(t),n_I(t),n_Q(t)} \, V_{DD}, \tag{3.14a}$$

$$y(t) = \mathbf{E} \, \mathbf{z}(t). \tag{3.14b}$$

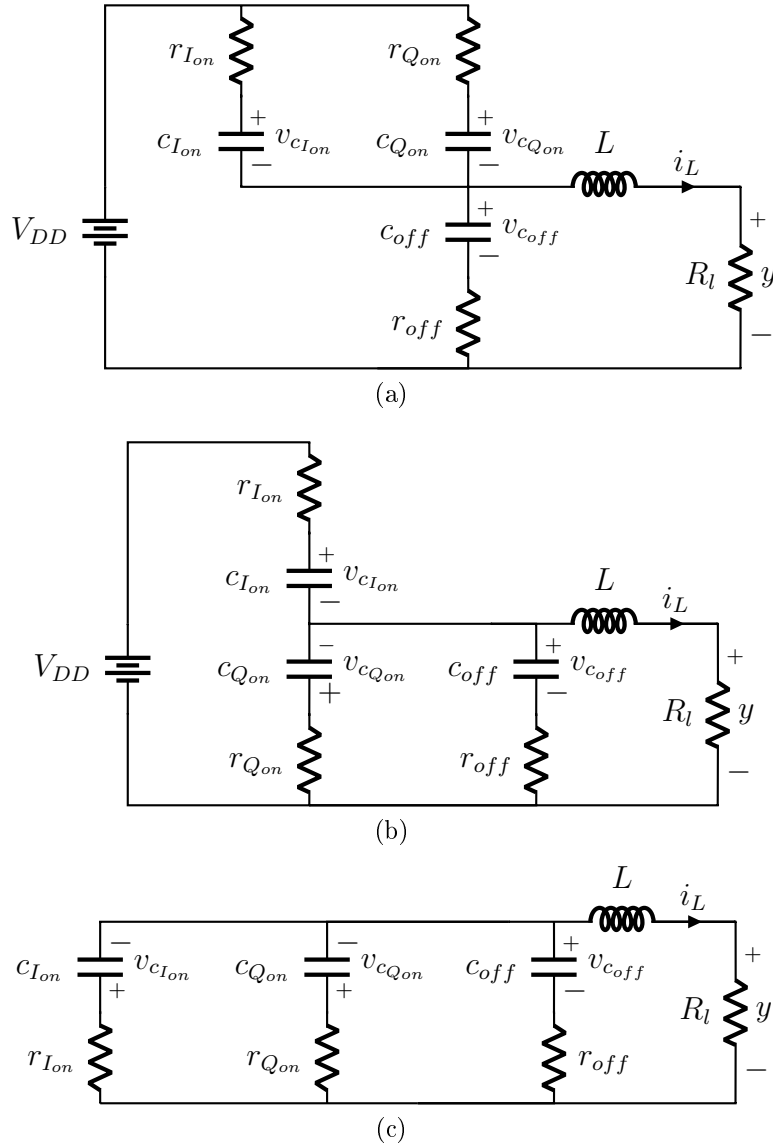State-space matrices are shown in Appendix B.2.

(a)

(b)

(c)

Figure 3.6: Equivalent circuits of the quadrature capacitive RF-DAC for (a) $\sigma_I(t) = 0$ and $\sigma_Q(t) = 0$, (b) $\sigma_I(t) = 0$ and $\sigma_Q(t) = 1$, and (c) $\sigma_I(t) = 1$ and $\sigma_Q(t) = 1$.

3.3 Extension to Switched Nonlinear State-Space Model

3.3.1 Circuit Theory

Circuit Model

Recalling the ideal schematic in Fig. 2.2, n parallel active unit-cells are connected in series with $(N - n)$ parallel inactive cells. When taking the switch parasitics from Section 3.2.1 into account, an effective on-resistance of $r_{\text{on}} = \frac{r_{\text{on,n/p}}}{n}$ for active and $r_{\text{off}} = \frac{r_{\text{on,n}}}{(N-n)}$ for inactive cells can be derived. Similarly, the parasitic diffusion

55

capacitance scales with n for active and $(N - n)$ for inactive cells, respectively. Semi-ideal switches toggle complementary between supply and ground to (dis-)charge the capacitive array (without matching network) with impedance

$$Z_{in} = \frac{1}{j\omega C_u} \cdot \left[\frac{N}{n(N-n)} \right],$$ (3.15)

which is dependent on the number of active cells n and thus on the input signal $\tilde{x}(t)$. However, the on-resistance of a CMOS transistor is strongly nonlinearly dependent on the drain-source voltage $|V_{ds}|$. The simulation results for a given PMOS/NMOS channel geometry are plotted in Fig. 3.7a. Likewise, the transistor diffusion capacitances are sketched in Fig. 3.7b.
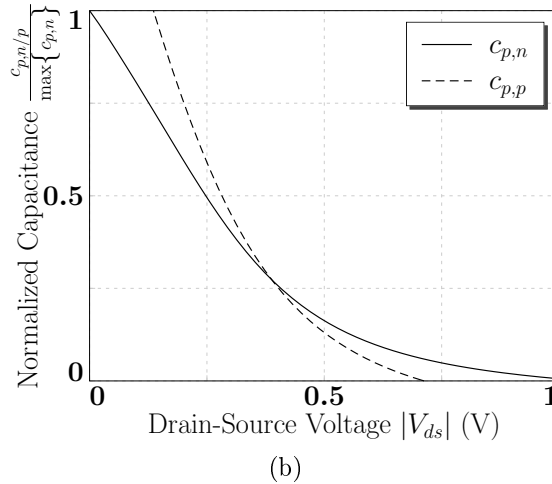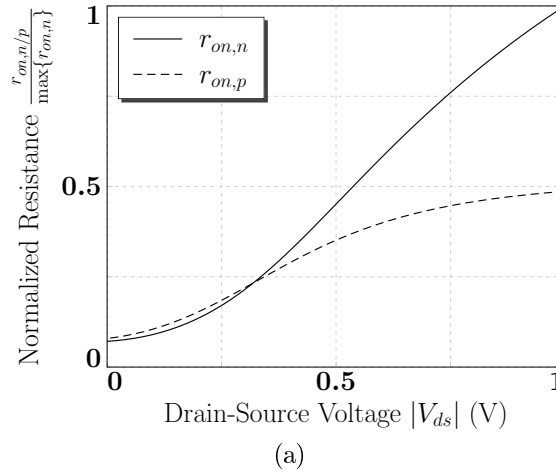

(a)

(b)

Figure 3.7: Simulated inverter performance for $W_P \approx 2 \cdot W_N$. (a) Channel on-resistance. (b) Diffusion capacitance.

When properly choosing the PMOS/NMOS channel geometry, the on-resistance of both devices is approximately equal for low $|V_{ds}|$. However, the difference increases as the drain-source voltage increases. Thus for large $|V_{ds}|$, the assumption

of equal NMOS/PMOS channel resistances is not valid anymore. For the accumulated drain capacitance the situation is slightly different: there is hardly a difference between NMOS $c_{p,n}$ and PMOS $c_{p,p}$ for large $|V_{ds}|$. The difference increases as the drain-source voltage decreases.

Since the switch parasitics depend on the drain-source voltage, which in turn changes over time and input code as shown in (2.5), all lumped components are variable. This leads to the nonlinear circuit model shown in Fig. 3.8.
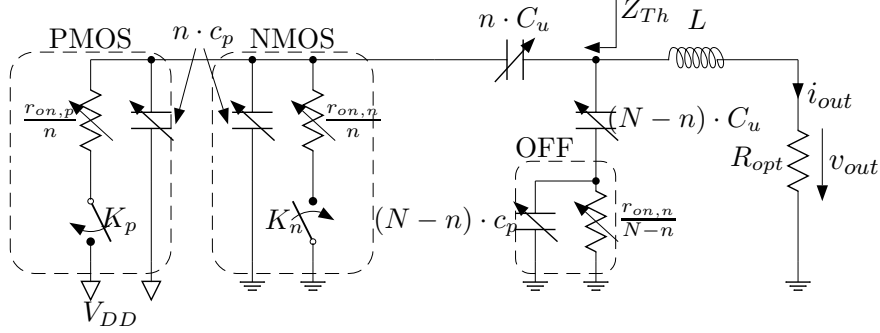

Figure 3.8: Single-ended series RLC circuit using varistors and variable capacitors as a nonlinear capacitive RF-DAC circuit model.

Similar to the ideal circuit, the Thévenin equivalent impedance seen from the OMN into the nonideal RF-DAC array is

$$Z_{Th} = \frac{\omega C_u \left((r_{\mathrm{ON}} \cdot r_{\mathrm{OFF}}) - \frac{1}{\omega^2 C_u^2} \right) - \mathrm{j}\,(r_{\mathrm{ON}} + r_{\mathrm{OFF}})}{\omega C_u \left((N-n)\, r_{\mathrm{ON}} + n\, r_{\mathrm{OFF}} \right) - \mathrm{j}\, N}. \tag{3.16}$$

with $r_{\mathrm{ON}} = \frac{r_{\mathrm{on,p/n}}}{n}$ and $r_{\mathrm{OFF}} = \frac{r_{\mathrm{on,n}}}{N-n}$ The parasitic capacitance c_p is in the order of tens of fF for e.g. a 28nm process and has thus been neglected.

An important characteristic can be obtained from (3.16): in presence of PMOS/NMOS on-resistance the output impedance becomes code dependent if and only if the charging and discharging networks are unequal. Thus for equal on-resistances of the PMOS/NMOS transistors, there will be no code-dependent phase shift since (3.16) will not be a function of n anymore. In other words, in case of $r_{\mathrm{on,n}} \neq r_{\mathrm{on,p}}$, both magnitude and phase of Z_{th} change with the number of active cells n, thereby causing code-dependent AM-PM distortion as will be described in the next section. This can be explained by the time-constant τ_{on} for the charging and τ_{off} for the discharging network:

$$\tau_{\mathrm{on}} = \frac{r_{\mathrm{on,p/n}}}{n} \cdot n\; C_u = r_{\mathrm{on,p/n}} \cdot C_u, \tag{3.17a}$$

$$\tau_{\mathrm{off}} = \frac{r_{\mathrm{on,n}}}{N-n} \cdot (N-n)\; C_u = r_{\mathrm{on,n}} \cdot C_u, \tag{3.17b}$$

which is an indicator for the delay of the signal at the output. The time-constants are equivalent only if the respective on-resistances are equivalent, i.e. $\tau_{\mathrm{on}} = \tau_{\mathrm{off}}$ only if $r_{\mathrm{on,p}} = r_{\mathrm{on,n}}$.

3.3.2 Origin of AM-AM and AM-PM Distortions

Figure 3.9 depicts the fundamental current/voltage waveforms of an ideal RF-DAC unit cell (solid lines) with attached OMN and shows the effect of increasing NMOS/PMOS on-resistance (dashed lines).

The transient behavior of the circuit can be analyzed by breaking the operation cycle into two phases. In each phase, one transistor is switched on while the other is off. Thus in the high (low) state of the LO signal, the NMOS (PMOS) device is active and contributes to imperfections caused by its parasitic elements. This results in a switch voltage of

$$v_C\left(t\right) = v_{DD}\left(t\right) \pm I_o \cdot r_{\mathrm{on,n/p}} \cdot \sin\left(\omega_0 t\right),\tag{3.18}$$

where

$$v_{DD}\left(t\right) = \begin{cases} V_{DD}, & \text{when LO is low} \\ 0, & \text{when LO is high.} \end{cases}\tag{3.19}$$

The current flowing through an ideal active device is a half-sinusoidal waveform without any distortion. The half-sinusoidal waveform is a result of the filtering caused by the connected output matching network. From the nonlinear circuit model, the drain current for NMOS/PMOS is given by

$$i_{\mathrm{on,n/p}}\left(t\right) = \alpha\left(\frac{1}{\pi} + \frac{1}{2}\sin\left(\omega_0 t\right) - \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{\cos\left(2k\,\omega_0 t\right)}{4k^2-1}\right),\tag{3.20}$$

where

$$\alpha = \frac{V_{DD}}{R_{opt}} \cdot \frac{n}{N} \cdot \left(\frac{1}{1+\frac{r_{\mathrm{on,n/p}}}{R_{opt}}}\right).\tag{3.21}$$

In presence of a parasitic on-resistance the respective drain current $i_{\mathrm{on,n}}\left(t\right)$ and $i_{\mathrm{on,p}}\left(t\right)$ show a reduced amplitude I_o and shifted zero-crossing as the on-resistance increases. Interestingly α varies if $r_{\mathrm{on,n}} \neq r_{\mathrm{on,p}}$ which means that asymmetric on-resistances of the PMOS and NMOS transistors translate into a distortion of the output current transient zero-crossing point i_{out}, which is shown in Fig. 3.10. The ratio $\varrho = \frac{r_{\mathrm{on,n}}}{r_{\mathrm{on,p}}}$ describes the level of mismatch between the active devices. While for $\varrho = 1$ the current crosses zero at exactly $\omega_0 t = 2\pi$, a shift of the zero-crossing results from $\varrho \neq 1$. This effect results in a phase distortion in the overall circuit.

Moreover, the ratio between device on-resistance and load resistance also affects the current flowing through the active device in case of nonzero on-resistance. Hence, for small load resistances, the effect of AM-PM distortion is exacerbated as can be seen in (3.21). In Fig. 3.10, the absolute value of $r_{\mathrm{on,n/p}}$ determines the slope at the zero-crossing but it has no impact on the AM-PM distortion as long as $\varrho = 1$ [30].
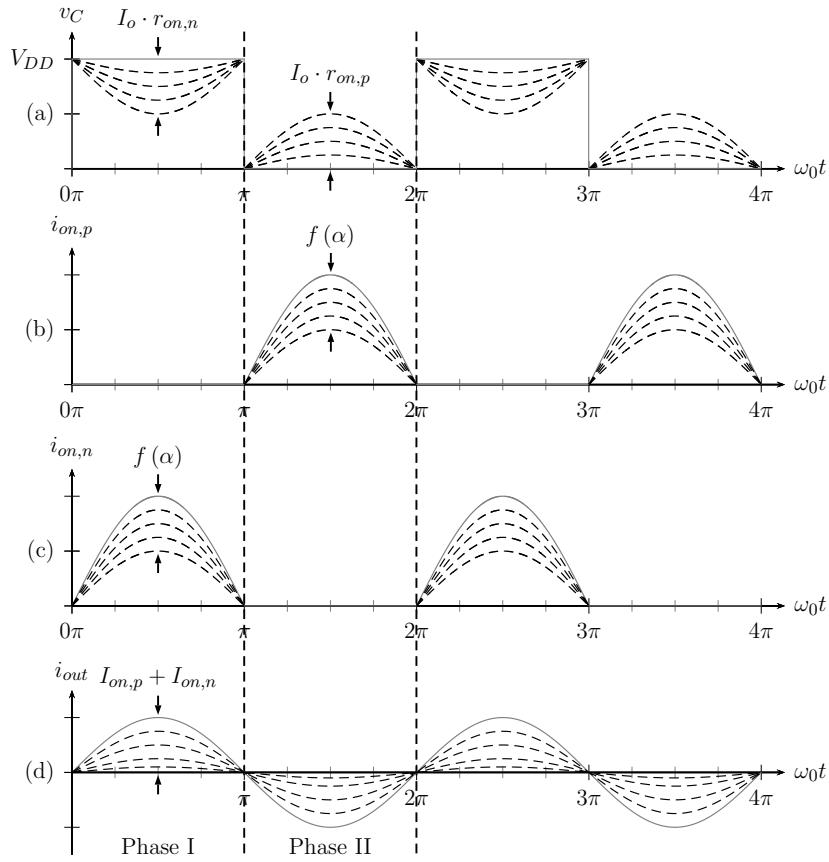
Figure 3.9: Current/voltage waveforms for a RF-DAC unit-cell with OMN, with (a) switch voltage, (b) capacitor charging current, (c) capacitor discharging current, and (d) output current waveform.
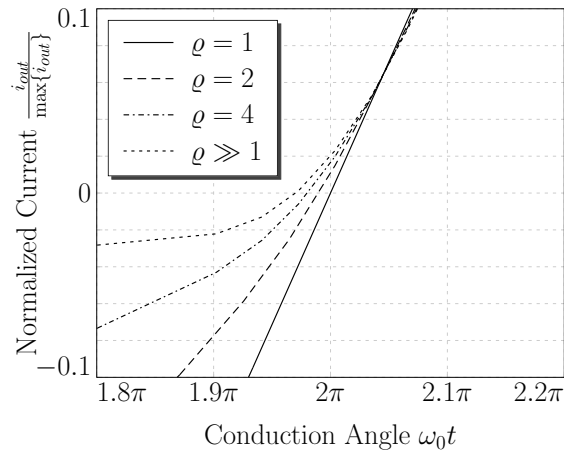

Figure 3.10: Shift of zero-crossing caused by asymmetric on-resistance as an indicator for the origin of AM-PM distortion in RF-DAC circuits.

3.3.3 Switched Nonlinear State-Space Model

This section extends the switched linear state-space model to switched nonlinear state-space models (NSSM), where each subsystem is described by a set of nonlinear differential equations.

As shown in (3.20) and (3.21), the phase distortion of the overall circuit depends on the ratio between the on-resistances of the NMOS and PMOS transistors. Figure 3.11 shows the evaluated AM-PM distortion for the switched LSSM and SpectreRF® simulations of a 28nm quadrature capacitive RF-DAC. It can be seen that with equal on-resistances there is no AM-PM distortion and the capacitive RF-DAC behaves almost linear as expected from (3.20). With different, but constant on resistances, a linear AM-PM distortion is introduced. However, when compared with the SpectreRF® simulation, the switched LSSM still shows a mismatch, resulting from the described dynamic behavior of the on-resistances of the transistors. Henceforth, modeling the inverter stage with different, but static on-resistances as with the switched LSSM approach does not cover all of the generated AM-PM distortions. Therefore, the switched state-space modeling concept is extended to include the dynamic behavior of the on-resistances $r_{\mathrm{on,n}}$ and $r_{\mathrm{on,p}}$, depending on the varying drain-source voltage $|V_{DS}(t)|$. Without loss of generality, the following uses the time-discrete form of the switched state-space model.
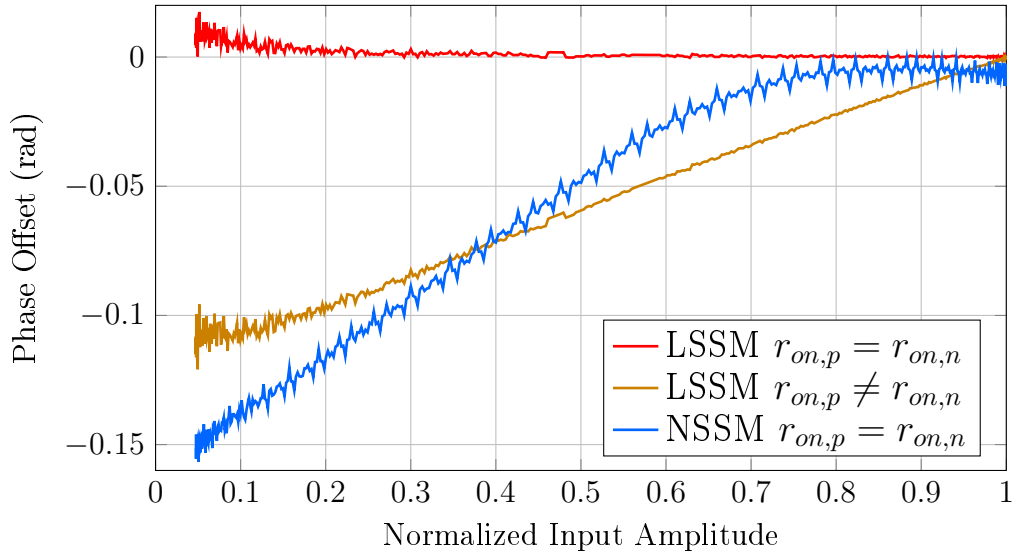

Figure 3.11: AM-PM comparison of the switched LSSM and NSSM simulations for a 28 nm quadrature capacitive RF-DAC.

In (3.4a), the state vector for the discrete time step $k+1$ is described by the linear mappings $\{\mathbf{A}_d, \mathbf{B}_d\}_{\Sigma[k]}$. Here, the switching signal $\Sigma[k]$ for the polar architecture is composed of the defined LO switching signal $\sigma[k]$ and the number of active switching cells $n[k]$ as in (3.9a). For the quadrature architecture $\Sigma[k]$ is composed of the quadrature LO signals $\sigma_I[k], \sigma_Q[k]$ and the number of active in-phase and quadrature cells $n_I[k], n_Q[k]$, respectively, as given in (3.14a).

By knowing the state vector $\mathbf{z}[k+1]$ also the drain-source voltages for each equivalent on-resistance can be calculated. These values are then used for the next time step $k+1$, i.e. $|V_{DS}|[k+1] = f(\mathbf{z}[k+1])$, respectively. The discrete transition of the state vector from time instant k to $k+1$ is determined by $\mathbf{A}_{d_{\Sigma}[k]}$ and $\mathbf{B}_{d_{\Sigma}[k]}$, where the elements of the new state vector $\mathbf{z}[k+1]$ are the voltages over the capacitors and the current through the inductor at time instant $k+1$. The drain-source voltages of the on-resistances can then be calculated by using Kirchhoff's voltage and current laws for the equivalent circuits shown in Figure 3.5 or Figure 3.6, i.e.

$$V_{DS,r_{\text{on,p}}}[k+1] = f_1(\mathbf{z}[k+1]), \tag{3.22a}$$

$$V_{DS,r_{\text{on,n}}}[k+1] = f_2(\mathbf{z}[k+1]), \tag{3.22b}$$

where f_1 and f_2 denote the linear equations to calculate the drain-source voltages for the active NMOS and PMOS devices.

The following equations for $|V_{DS}|[k+1]$ and $r_{\text{on}}[k+1]$ are derived for the polar architecture only, but can be similarly used for the quadrature architecture. The calculated drain-source voltages for the on-resistances in (3.7c) and (3.7d) are equal for all individual parallel active and passive unit cells, respectively. Therefore, to calculate $|V_{DS}|[k+1]$, the following set of equations must be solved:

$$V_{DS,p} = u - v_{c_{\text{on}}} - v_{c_{\text{off}}} - V_{DS,n}, \tag{3.23a}$$

$$I_{DS,p} = i_L - I_{DS,n}, \tag{3.23b}$$

$$I_{DS,p} = \beta_p(V_{DS,p}), \tag{3.23c}$$

$$I_{DS,n} = \beta_n(V_{DS,n}), \tag{3.23d}$$

where u is either V_{DD} or V_{SS}, depending on the state of the switching signal. The parameters of the polynomials β_{PMOS} and β_{NMOS} have been fitted to the measurement results shown in Figure 3.7 with a least-squares approximation in MATLAB. As shown in (3.8), the variables $v_{c_{\text{on}}}$, $v_{c_{\text{off}}}$ and i_L are elements of the state vector $\mathbf{z}$. The functions β_p and β_n are polynomials, which map the drain-source voltage to the drain-source current in dependency of the on-resistance as shown in Figure 3.7a for PMOS and NMOS transistors, respectively. Since β_p and β_n are nonlinear functions, the unit on-resistances inherently show a nonlinear dependency on the internal state vector $\mathbf{z}$ of the capacitive RF-DAC. Furthermore, the switching signal state $\sigma[k+1]$ must be known for the next circuit configuration such that $r_{\text{on/off}}[k+1]$ is calculated for the PMOS or the NMOS transistors, respectively. The resulting on-resistances r_{on} and r_{off} are then used in the derivation of the system matrices $\mathbf{A}_{m,n}$ and $\mathbf{B}_{m,n}$ for the discrete-time step $k+1$:

$$\mathbf{A}_{0,n}[k+1] = \begin{bmatrix} -\frac{1}{c_{\text{on}} \cdot r_t} & -\frac{1}{c_{\text{on}} \cdot r_t} & 1-\frac{r_{\text{on,p}}}{c_{\text{on}} \cdot r_t} \\ -\frac{1}{c_{\text{off}} \cdot r_t} & -\frac{1}{c_{\text{off}} \cdot r_t} & -\frac{r_{\text{on,p}}}{c_{\text{off}} \cdot r_t} \\ -\frac{r_{\text{off}}}{L \cdot r_t} & 1-\frac{r_{\text{off}}}{L \cdot r_t} & -\left(\frac{R_L}{L}+\frac{r_{\text{on,p}} \, r_{\text{off}}}{L \cdot r_t}\right) \end{bmatrix}, \tag{3.24a}$$

$$\mathbf{B}_{0,n}[k+1] = \begin{bmatrix} \frac{1}{c_{\text{on}} \cdot r_t} \\ \frac{1}{c_{\text{off}}} \\ \frac{r_{\text{off}}}{L \cdot r_t} \end{bmatrix}, \tag{3.24b}$$

where $r_t = r_{\mathrm{on,p}} + r_{\mathrm{off}}$. Similar relations hold for $\sigma[k] = m = 1$. With the dependency of the equivalent resistors r_{on} and r_{off} for simulation step $k+1$ on the internal states of the system, also $\mathbf{A}_{m,n}[k+1]$ and $\mathbf{B}_{m,n}[k+1]$ become nonlinearly dependent on the internal vector $\mathbf{z}[k]$. Thus, the system can no longer be described by linear state-space equations and is therefore extended to the nonlinear state-space model:

$$\mathbf{z}[k+1] = \mathbf{h_A}\left(\mathbf{z}[k]\right)\mathbf{z}[k] + \mathbf{h_B}\left(\mathbf{z}[k]\right)\mathbf{u}[k], \qquad (3.25\mathrm{a})$$

$$\mathbf{y}[k] = \mathbf{E}\,\mathbf{z}[k], \qquad (3.25\mathrm{b})$$

where $\mathbf{h_A}(\cdot)$ and $\mathbf{h_B}(\cdot)$ depict the state-space matrices with the nonlinear dependency on the state vector $\mathbf{z}$. The output is the same as in (3.9b).

To calculate the respective entries of the state dependent matrices $\mathbf{h_A}\left(\mathbf{z}[k]\right)$ and $\mathbf{h_B}\left(\mathbf{z}[k]\right)$ the NSSM approach requires the system to be in a stable state between two consecutive sampling steps. To fulfill this requirement, and to include the dynamic behavior of the inverter also in the switching transition, a high over-sampling ratio is required when compared to the switched LSSM. With that, the particular state changes during the small sampling period are negligible. As a result the required absolute simulation run-time is higher when compared to the switched LSSM but still significantly faster than a transistor-level simulation using SpectreRF®.

The proposed principle is also valid for varying (nonideal) rising and falling edges of the LO signal as the on-resistances are calculated for each simulation step. With that, the NSSM is also valid during the transition phases of the driving LO signal. Moreover, the proposed state-space modeling concept can even be simulated with varying sampling rates, i.e. a higher sampling rate can be used for the transition phases (rising and falling edges) of the LO signal and a lower sampling rate for the (relatively) long on and off phases of the LO signal, respectively. This reduces the required simulation run time. As will be shown in the following, the acquired accuracy of the NSSM is significantly increased over the LSSM by modeling the dynamic on-resistances.

3.3.4 Experimental Results

This section shows the simulation results of the proposed state-space models and validates them against results achieved by the circuit simulator SpectreRF® and measurements. Furthermore, a comparison to typically used equivalent baseband RF-PA behavioral models is presented.

Circuit Model Validation

Three types of circuit models are used to validate the proposed approach of the switched NSSM on a transistor-level:

1. The reference model is a transistor-level implementation of a 28 nm CMOS capacitive RF-DAC simulated with SpectreRF®. All active devices utilize state-of-the-art transistor models [98].

2. Switched LSSM with static on-resistances.

3. Switched NSSM including the dynamical behavior of the CMOS transistors.

Basic circuit parameters are given in Table 3.1. The switched LSSM and NSSM are simulated with MATLAB/Simulink. All models are based on a 15-bit quadrature capacitive RF-DAC design. The LO frequency is set to $f_{LO} = 2\,\text{GHz}$. Each simulation setup uses equidistant sampling and quasi-ideal rising and falling edges of the LO signal. The drain-source currents and drain-source voltages of the PMOS and NMOS transistors, as shown in Fig. 3.7a, have been extracted from static DC simulations with SpectreRF® using the transistors of the reference model. The LSSM and NSSM are simulated with equal and unequal on-resistances to quantify the effect of applying the time- and code-dependent transistor on-resistances in comparison to static on-resistances.

Table 3.1: IQ C-DAC circuit parameters.

| Total array capacitance	20.48 pF
Number of bits	15
PMOS	$W = 420\,\text{nm}, L = 30\,\text{nm}$
NMOS	$W = 210\,\text{nm}, L = 30\,\text{nm}$
Supply voltage	1.1 V
LO frequency	2 GHz
Max. output power	14 dBm[1]

[1] CW input signal.

AM-AM and AM-PM behavior of the different modeling approaches have been extracted from simulations using static and dynamic input codes, whereas a 2 MHz complex single-tone input signal is used in the dynamic case.

The resulting AM-AM and AM-PM characteristics are shown in Fig. 3.12. In terms of AM-AM behavior, all configurations show almost the same result as sketched in Fig. 3.12a. The LSSM and the proposed NSSM with equal and unequal on-resistances show good matching when compared to the SpectreRF® simulation. The AM-PM behavior is shown in Fig. 3.12b. The LSSM with equal on-resistances shows no AM-PM distortion. Unequal on-resistances degrade the AM-PM behavior also for the LSSM, as predicted in (3.20) and (3.21). Anyhow, the LSSM still shows a significant deviation from the SpectreRF® simulation results. The NSSM with unequal and dynamic on-resistances, on the other hand, achieves superior matching to the transistor level simulations. This shows that the dynamic behavior of the on-resistances has a significant impact on the AM-PM distortion and should, therefore, be considered when modeling capacitive RF-DACs.
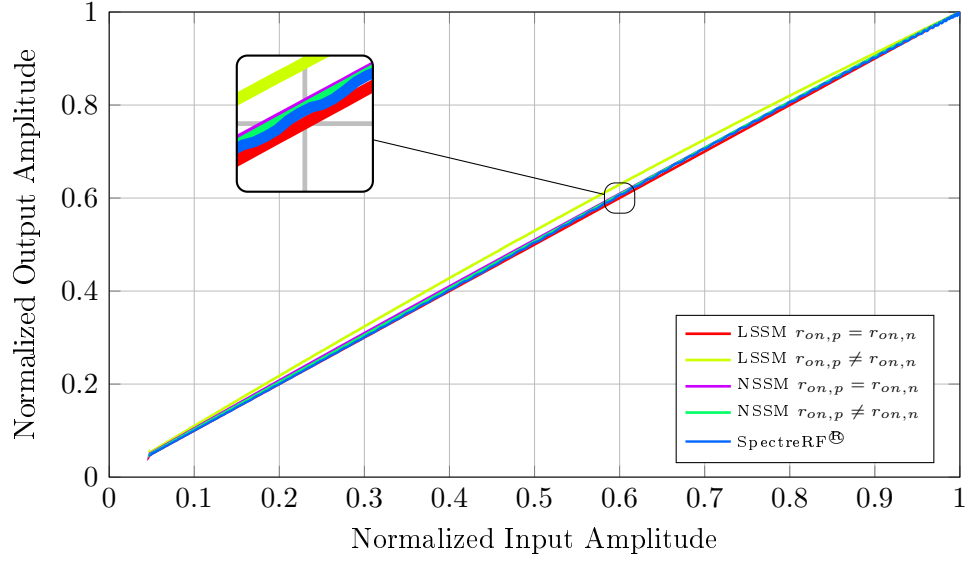
(a)
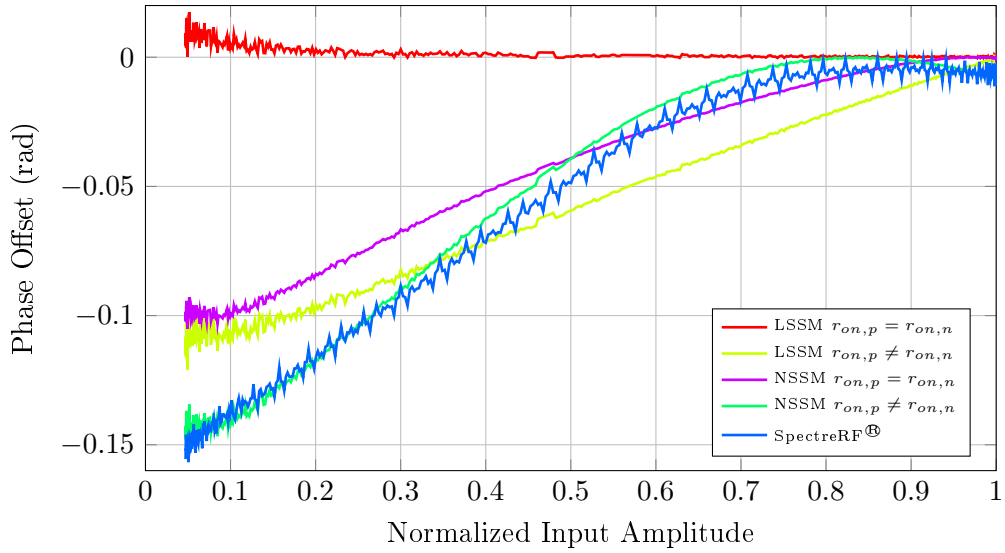
(b)

Figure 3.12: Comparison of AM-AM and AM-PM behavior between SpectreRF®, LSSM and NSSM. (a) AM-AM response. (b) AM-PM response.

Performance Validation Against Measurements and Behavioral Models

In extension to the circuit level validation, the proposed NSSM is also compared to RF-PA behavioral models and validated against measurement results. The chosen models are equivalent baseband models, including the Hammerstein model, Rapp's model, and Saleh's model [35, 61, 62, 99, 100], as described in Section 2.2.2.

The measured RF-DAC is a quadrature capacitive RF-DAC manufactured in a 28 nm CMOS process. A chip micro-photograph of the capacitive RF-DAC

and the measurement setup are shown in Fig. 3.13 and Fig. 3.14, respectively. The digital input signal samples are generated with MATLAB and transferred to the capacitive RF-DAC test chip with a vector signal generator, which generates the required in-phase and quadrature signals $x_I(t)$ and $x_Q(t)$. The RF output signal of the capacitive RF-DAC $y(t)$ is measured and demodulated by a signal analyzer. The resulting equivalent digital baseband samples $\tilde{y}(kT_s)$ are loaded to the PC/MATLAB environment for post-processing (EVM, FFT).
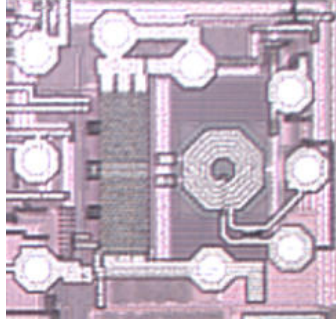
Figure 3.13: Micro-photograph of the 28 nm manufactured IQ capacitive RF-DAC.
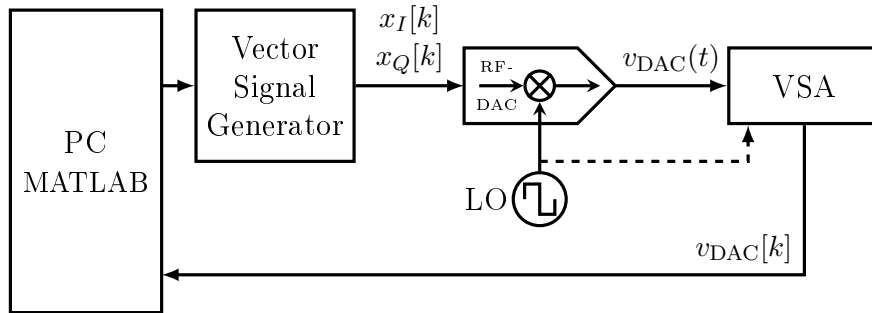
Figure 3.14: Measurement setup for measuring an on-chip CMOS capacitive RF-DAC for comparison with the proposed models.

Fig. 3.15 shows the estimated PSDs of the capacitive RF-DAC's output signal for the measurement results and the chosen models. Again, a complex single-tone signal with $f_{sig} = 2\,\text{MHz}$ was chosen as an input signal to easily distinguish the performance of the chosen models for specific nonlinear characteristics. Single-tone measurements are frequently used to analyze the non-linear behavior of data converters as the frequency of the resulting harmonics are easily calculated and visualized in frequency domain plots.

The equivalent baseband models (Hammerstein, Rapp, Saleh) only show a minor coverage of the spurious elements in the output signal spectrum. The Hammerstein model was fitted using the down-converted output data of the quadrature RF-DAC using a wideband input signal. Rapp and Saleh parameters have been extracted from sinusoidal input signals. The switched NSSM approach, on the other hand, shows quite a good matching to the simulation results from SpectreRF®. Disagreement between SpectreRF® and measurements are mainly due to nonideal

effects of the supply and matching networks, respectively, which are not covered in this section. Detailed results of the intermodulation distortions (IMDs) caused by the nonlinear characteristics of the capacitive RF-DAC are given in Table 3.2. The NSSM achieves good results for upper and lower IMDs compared to SpectreRF® simulations and outperforms the state-of-the-are PA models. Moreover, the performance of the behavioral models is strongly limited for far out-of-band signal regions, whereas the NSSM shows good matching with SpectreRF® simulations and measurement results as can also be seen in Fig. 3.15.

Additionally, extended simulations with an LTE-Advanced (256-QAM) modulated input signal, composed of two component carriers with aggregated bandwidth of 40 MHz have been performed. The corresponding constellation diagrams, normalized to the LSB of the capacitive RF-DAC, for each model and the measurement results are presented in Fig. 3.16.

The estimated PSDs of the input signal and the capacitive RF-DAC's output signal for the LSSM, NSSM, SpectreRF® and measurements are shown in Fig. 3.17. For better visibility, the spectrum plot only shows the switched state-space models, the reference model's output, and the measurement results. The resulting EVM results are listed in Table 3.2, where the NSSM outmatches the behavioral models and achieves a 0.7 % matching with SpectreRF® simulations and measurement results.

Another important characteristic of the different modeling possibilities is the required simulation run time. The switched NSSM is more than 50 times faster than the SpectreRF® transistor level model. Although the PA behavioral models are much faster, their accuracy is very limited, especially for the far out-of-band signal region. Furthermore, these models lack possibilities to model distinct nonidealities as discussed in the next section.

3.4 Modeling of Other Non-ideal Effects with Switched State-Space Models

This sections discusses the possibilities to add dedicated non-ideal effects to the switched state-space modeling approach. To differ and study the impact of different effects the switched LSSM is chosen, which allows to model an ideal capacitive RF-DAC by keeping on-resistances equivalent $r_{\text{on,p}} = r_{\text{on,n}}$. Consequently the resulting effects of distinct non-idealities on the output of the RF-DAC can be easily analyzed. Nevertheless, all of the mentioned modeling concepts below can also be applied to the switched NSSM approach.

3.4.1 Cell Mismatch

Component variations are a fundamental problem of integrated circuits. The unavoidable deviations in the manufacturing process result in parameter variations
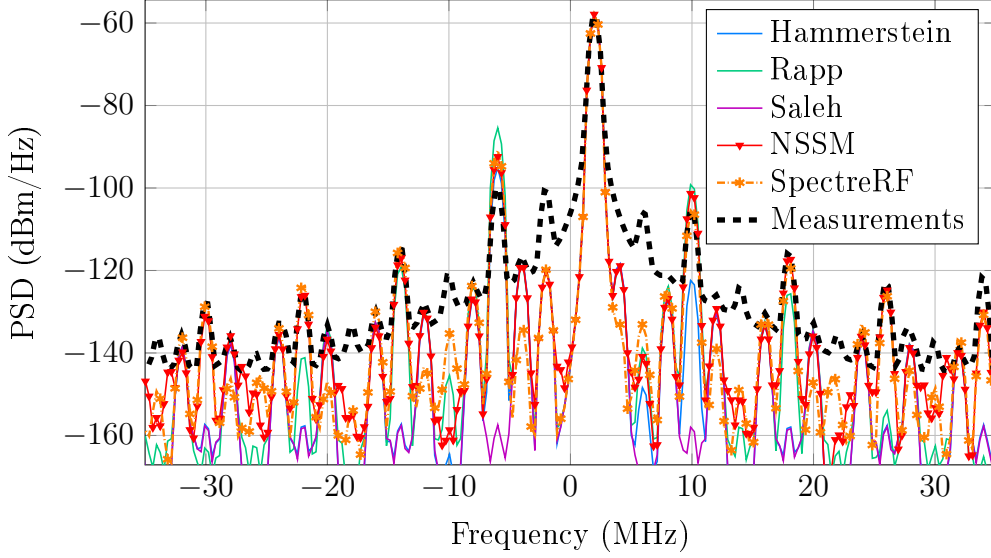
Figure 3.15: Estimated PSDs of the equivalent baseband signals of the quadrature capacitive RF-DAC output for NSSM, SpectreRF®, measurements, and chosen behavioral models for a complex single-tone input signal with 2 MHz.

and mismatch between devices and structures that should ideally be equal, effecting the performance of the circuitry.

The capacitive RF-DAC is composed of an array of matched unitary cells [30,42]. However, due to the phenomenon of manufacturing variations, the driving inverters and especially capacitors in the matched cells slightly deviate from their ideal values. The output voltage of the capacitive RF-DAC is thus no longer described simply by the ratio of active cells to the number of total cells $\frac{n(t)}{N}$ as in (2.6). Accounting for capacitor mismatch results in

$$v_{\text{DAC}}(t) = \frac{2}{\pi} \, V_{\text{DD}} \, \frac{\sum_{i=1}^{n} C_u + \Delta C_i}{\sum_{i=1}^{N} C_u + \Delta C_i} \, \sin\left(\omega_{\text{LO}}t\right), \tag{3.26}$$

where ΔC_i is the respective deviation of the i-th unit cell from its ideal value C_u. This deviation is typically modeled by a zero-mean Gaussian process, i.e. $\Delta C_i \sim \mathcal{N}\left(0, \sigma_C^2\right)$, which depends on the capacitor size and process parameters.

The effect of device mismatch is typically evaluated by Monte Carlo simulations, i.e. a large number of individual runs with varied component parameters, requiring immense computational efforts when using circuit level simulators. The capacitor mismatch can directly be integrated in the switched LSSM approach. The respective on and off capacitance values, accounting for mismatch, are calculated as

$$c_{\text{on}} = \sum_{i=1}^{n} C_u + \Delta C_i \qquad\qquad c_{\text{off}} = \sum_{i=n+1}^{N} C_u + \Delta C_i \tag{3.27}$$

where for an ideal implementation, i.e. $\Delta C_i = 0$, the on and off values become again $c_{\text{on}} = n \, C_u$ and $c_{\text{off}} = (N - n) \, C_u$, respectively.
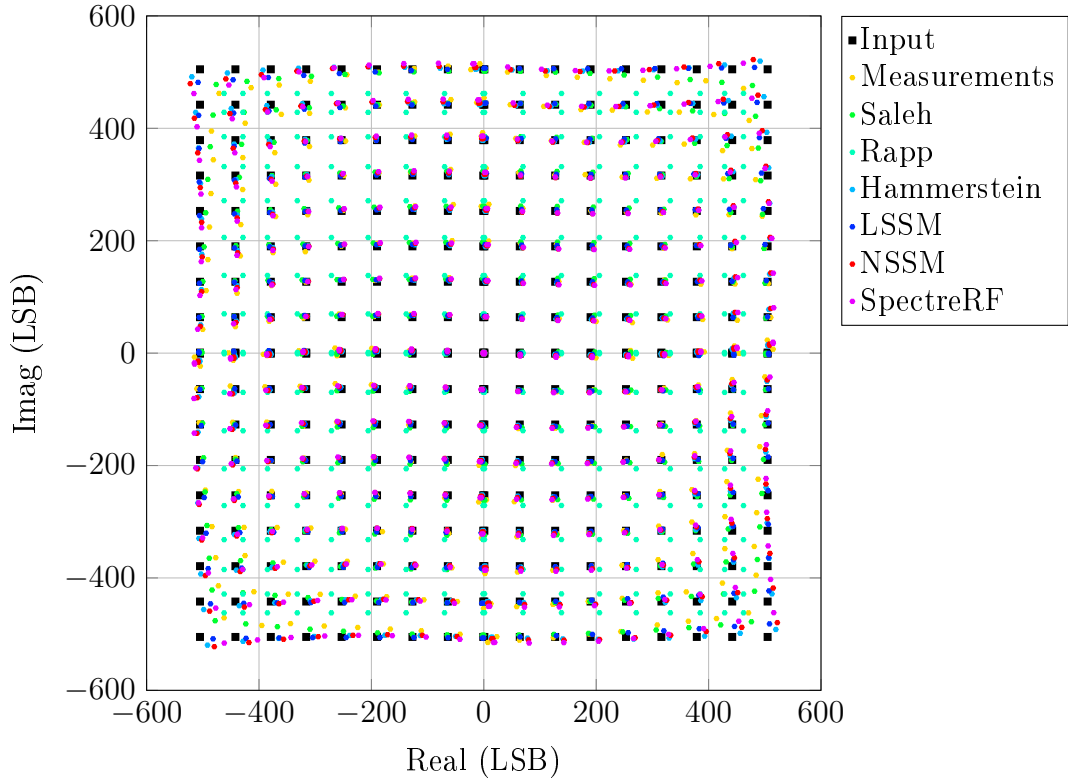
Figure 3.16: Constellation diagram of the different models and measurement results for a 256-QAM modulated LTE signal normalized to the LSB of the capacitive RF-DAC.

This approach provides a computationally efficient and fast way to simulate the performance degradation of the capacitive RF-DAC for dedicated mismatch in transient simulations. Figure 3.18 shows the result of a mismatch for a multi-tone signal in a polar capacitive RF-DAC architecture using the switched LSSM. A Monte Carlo simulation is performed with 100 realizations of ΔC_i. The figure depicts the average over the individual PSDs.

3.4.2 Clock Jitter

Jitter and phase noise performance is a critical aspect of wireless transmitters. This is especially true for RF-DAC based architectures, where the LO acts as the sampling clock and upconverts the signal simultaneously. There are many undesired effects related to phase noise in communication systems, such as receiver desensitization, spectral mask violations, and SNR and EVM degradation [101–103].

Therefore, early and fast evaluation of the impact of LO phase noise and jitter on the transmitter performance is crucial for the design process. Circuit simulators can provide such analysis, but at the cost of severely increased simulation run times.

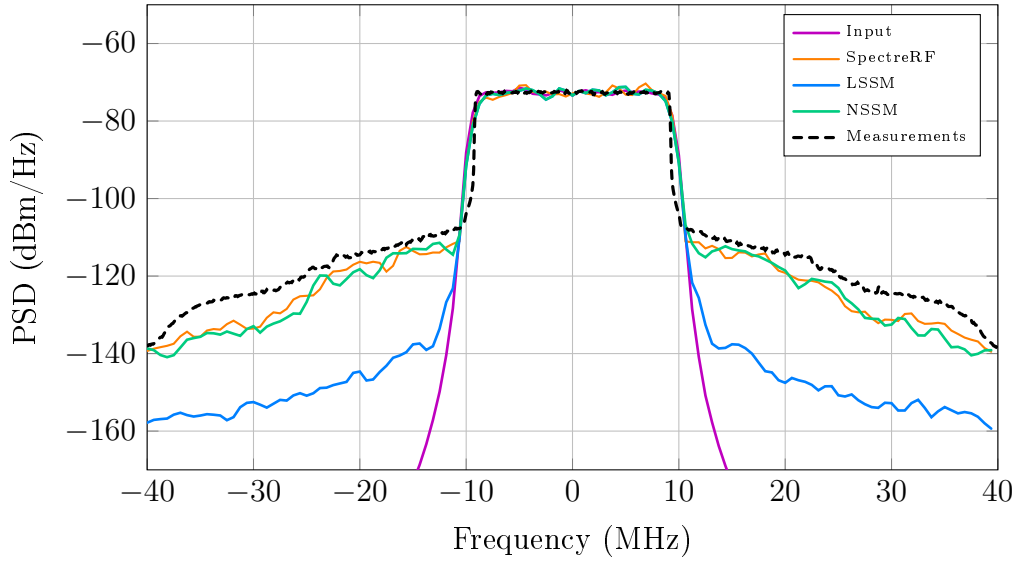Simplified models exist to analyze the effects of jitter on DACs [104–107], but

Figure 3.17: PSDs of the input signal and the equivalent baseband signals of the IQ capacitive RF-DAC output for LSSM, NSSM, SpectreRF®, and measurements for an LTE input signal with a bandwidth of 20 MHz.

these models only consider the jitter effect alone and cannot be combined with other non-idealities into a single model.

The switched LSSM uses the LO as a switching signal $\sigma[k]$ to select the active subsystem. Thus, timing variations on the LO signal change the subsystem switching instants. Hence, simulating the effect of timing jitter is easily performed with the switched state-space model, providing fast evaluation while maintaining its low complexity. However, modeling the small time changes in the switching signal due to the clock jitter also requires a much higher oversampling ratio for the simulation, depending on the actual clock variations.

The model is first validated by comparing the LO phase noise, drawn in blue in Figure 3.19, to the output of the RF-DAC model at a constant input. The DAC is excited with the same LO signal, and, if scaled correctly, the two spectra match. Additionally, Figure 3.20 shows the effect of LO jitter for a modulated input signal for a polar capacitive RF-DAC architecture. As expected, the performance is significantly impaired by phase noise, clearly visible in the out-of-band emissions.

3.4.3 Supply Voltage Variations

The supply voltage of the capacitive RF-DAC is also its reference voltage, making it thereof very sensitive to variations on supply. Noise and distortions on the supply V_{DD} are directly modulated with the input and LO as it is described by (2.6). This causes spectral regrowth and impairs in-band performance. Consequently, this is a critical effect to be considered in a properly modeled RF-DAC. Details of supply voltage variation effects are covered in Chapter 4.

Apart from thermal noise, supply voltage variations are typically deterministic.

Table 3.2: Performance comparison of the chosen models and measurement results.

Model Type	t_{run} [1] s	CIM3 dBc/Hz	IM5 dBc/Hz	CIM7 dBc/Hz	IM9 dBc/Hz	EVM[2] %
Hammerstein	6.2	-95	-122	-157.2	-158.1	1.7
Rapp	5.7	-85	-99	-119.5	-125.7	4.4
Saleh	6.8	-157.5	-158	-157.1	-158.7	2.3
Linear SSM	86	-108.1	-109.3	-121.7	-122.1	1.4
Nonlinear SSM	492	-92.4	-101.5	-116.7	-117.7	3.9
Cadence	26 189	-90.4	-105.4	-114.8	-119.1	3.2
Measurement	-	-99.4	-105.5	-115.1	-115.9	3.8

[1] Time to simulate $10\,\mu s$ with a sampling frequency of $F_s = 128\,\text{GHz}$.
[2] EVM results for 256-QAM LTE signal.

This includes distortion by supply regulators, such as switching ripples of a DC-DC converter [108]. Furthermore, the input signal-dependent current drawn by the RF-DAC causes undesired nonlinear effects across any supply impedance and wiring.

A possibility to model these supply related effects are nonlinear models such as Volterra Series or Wiener-Hammerstein models [22, 35, 109]. But these require complicated coefficient estimation and are hard to integrate within the LSSM approach due to the feedback nature of the supply current.

Alternatively, these effects can easily be implemented in circuit simulators by directly using appropriate values of the circuit. However, doing so, further increases the required computational effort of circuit-level simulations. Additionally, the dynamics of the supply related circuitry and the one of the RF-DAC are in quite different frequency ranges, which render such simulations impracticable. E.g. a DC-DC voltage regulator operates in the MHz region, while the RF-DAC is operated with the LO in the several GHz range.

Another benefit of the switched state-space modeling approach is its capability to directly include the supply network in the circuit equations of the subsystems. Thus, component values can directly be used. This provides the possibility of fast and accurate evaluation of the supply network parameters and their influence on the RF-DAC performance. Independently, DC-DC voltage regulators and their distortions can also easily be added to the input supply voltage in the model.

The inclusion of the supply network in the system equations covers the effects of supply voltage variations on the output signal as well as the feedback from the current drawn by the RF-DAC. Essentially, the effects of the supply network
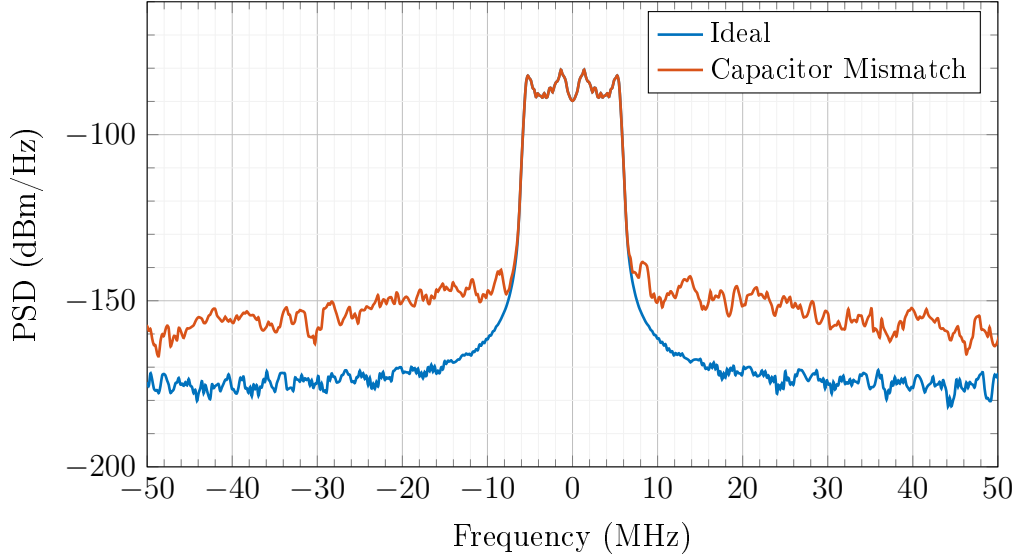
Figure 3.18: PSD of the downconverted RF-DAC output with capacitor mismatch for a multi-tone signal with $10\,\mathrm{MHz}$ bandwidth averaged over $n = 100$ runs.

can accurately be modeled, simulated, and analyzed. The state-space matrices for a polar capacitive RF-DAC, including an RLC supply network as shown in Figure 3.21 are given below

$$\mathbf{K}_{0,n} = \begin{bmatrix} L_s & 0 & 0 & 0 & 0 \\ 0 & C_s & 0 & 0 & 0 \\ 0 & 0 & c_n & 0 & 0 \\ 0 & 0 & 0 & c_{N-n} & 0 \\ 0 & 0 & 0 & 0 & L \end{bmatrix} \tag{3.28a}$$

$$\mathbf{A}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -Rs & \frac{-1}{1} & 0 & 0 & 0 \\ 1 & -\frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & \frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & \frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{r_{\mathrm{off}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} \\ 0 & \frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & \frac{r_{\mathrm{off}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} \\ 0 & \frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{1}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{r_{\mathrm{on}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} \\ 0 & \frac{r_{\mathrm{off}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{r_{\mathrm{off}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} & \frac{R_N}{r_{\mathrm{on}}+r_{\mathrm{off}}} & -\frac{R_l\,(r_{\mathrm{on}}+r_{\mathrm{off}})+r_{\mathrm{on}}\,r_{\mathrm{off}}}{r_{\mathrm{on}}+r_{\mathrm{off}}} \end{bmatrix} \tag{3.28b}$$

$$\mathbf{B}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{3.28c}$$

$$\mathbf{E}_{0,n} = \begin{bmatrix} 0 & 0 & R_l \end{bmatrix} \tag{3.28d}$$

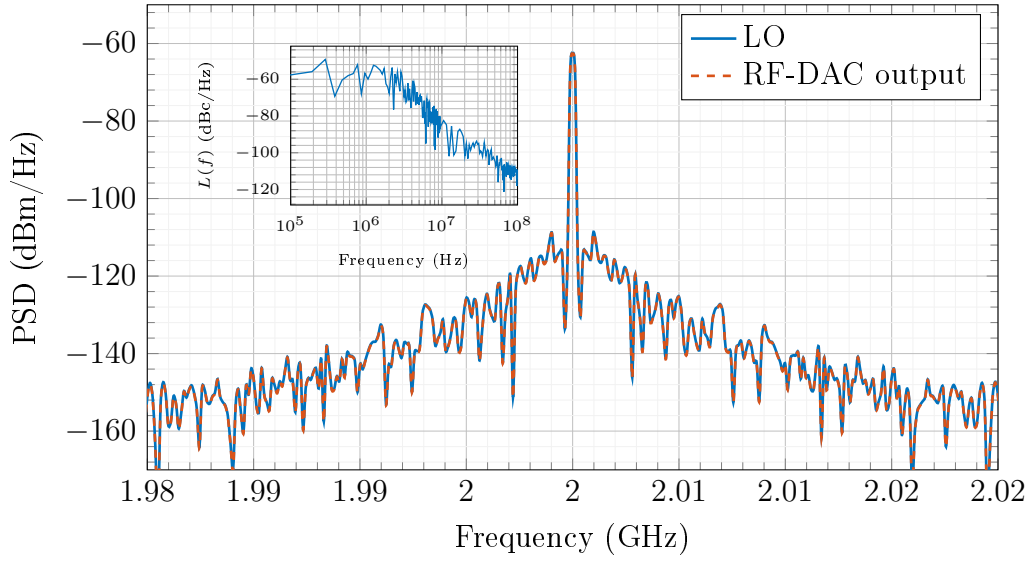$$\mathbf{F}_{0,n} = 0 \tag{3.28e}$$

Figure 3.19: PSD of the LO and (scaled) RF-DAC output with constant input code at $f_{\text{LO}} = 2\,\text{GHz}$. The phase noise spectrum of the applied LO, with $1\,\text{ps}$ RMS jitter, is shown in the small figure.

$$\mathbf{K}_{1,n} = \mathbf{K}_{0,n} \tag{3.29a}$$

$$\mathbf{A}_{1,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -Rs & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\dfrac{1}{r_{\text{on}}+r_{\text{off}}} & -\dfrac{1}{r_{\text{on}}+r_{\text{off}}} & \dfrac{r_{\text{off}}}{r_{\text{on}}+r_{\text{off}}} \\ 0 & 0 & -\dfrac{1}{r_{\text{on}}+r_{\text{off}}} & -\dfrac{1}{r_{\text{on}}+r_{\text{off}}} & -\dfrac{r_{\text{on}}}{r_{\text{on}}+r_{\text{off}}} \\ 0 & 0 & -\dfrac{r_{\text{off}}}{r_{\text{on}}+r_{\text{off}}} & \dfrac{R_N}{r_{\text{on}}+r_{\text{off}}} & -\dfrac{R_l\,(r_{\text{on}}+r_{\text{off}})+r_{\text{on}}\,r_{\text{off}}}{r_{\text{on}}+r_{\text{off}}} \end{bmatrix} \tag{3.29b}$$

$$\mathbf{B}_{1,n} = \mathbf{B}_{0,n} \tag{3.29c}$$

$$\mathbf{E}_{1,n} = \mathbf{E}_{0,n} \tag{3.29d}$$

$$\mathbf{F}_{1,n} = \mathbf{F}_{0,n} \tag{3.29e}$$

In contrast to the state-space equations of the polar model in (3.10b) and (3.11a), the system matrix structure changes with respect to the LO switching signal $\sigma[k]$. However, the input matrix $\mathbf{B}_{m,n}$ becomes independent of the LO as the supply network is always connected to V_{DD}.

Figure 3.22 shows the supply voltage for a sinusoidal input signal in a polar capacitive RF-DAC. With the LSSM also the high frequency switching disturbances on V_{DD} can be simulated as sketched in Figure 3.22. The spectrum of the RF-DAC output, including the effects of a supply network, is shown in Fig. 3.23.

3.4.4 Combining All Impairments

The impairments described above can be combined in a single simulation where again the required oversampling of the simulation must be chosen adequately to
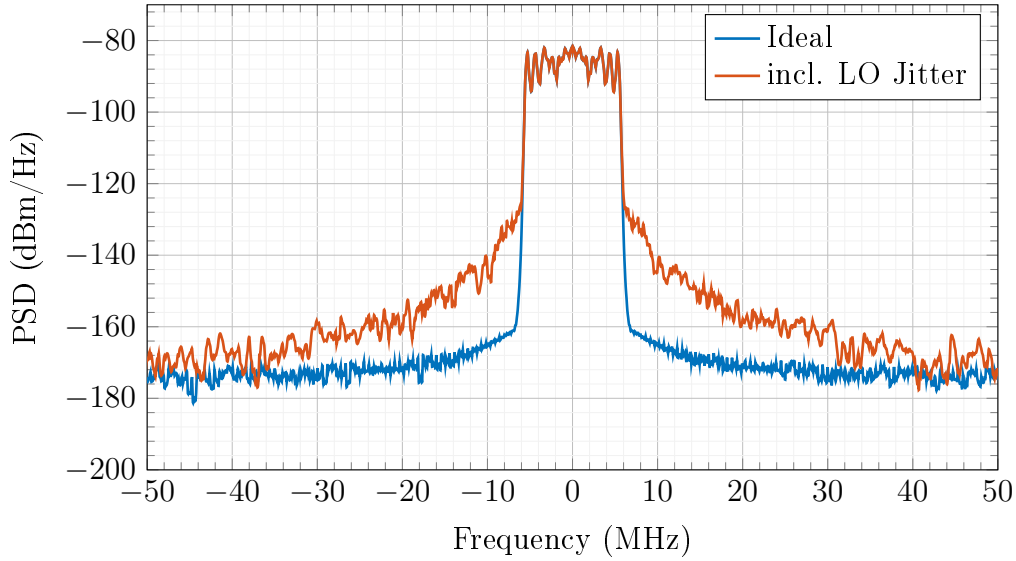
Figure 3.20: PSD of the downconverted RF-DAC output with ideal (blue) and non-ideal (red) LO for a 10 MHz bandwidth modulated signal.
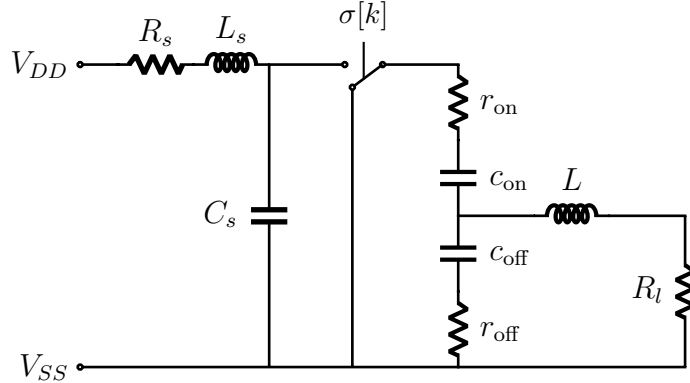

Figure 3.21: Simulated supply voltage variation including a supply network for a sinusoidal signal.

the required resolution of the LO jitter. The achieved overall simulation run-time benefit compared to standard SpectreRF® simulations is still almost a factor of 100, including all non-idealities.

Figure 3.24 shows the PSD of the RF-DAC output for a multi-tone input signal including capacitor mismatch, LO jitter, and a supply network. The supply network is composed of a passive series RLC circuitry, where the capacitor is parallel to the RF-DAC. The RMS clock jitter of the LO is 1 ps as in Figure 3.19.

Compared to Figures 3.18, 3.23, and 3.20, the spectrum shows significantly higher spectral regrowth. The near out-of-band distortions are dominated by the supply network of the RF-DAC and LO jitter. The far out-of-band noise is primarily determined by capacitor mismatch.
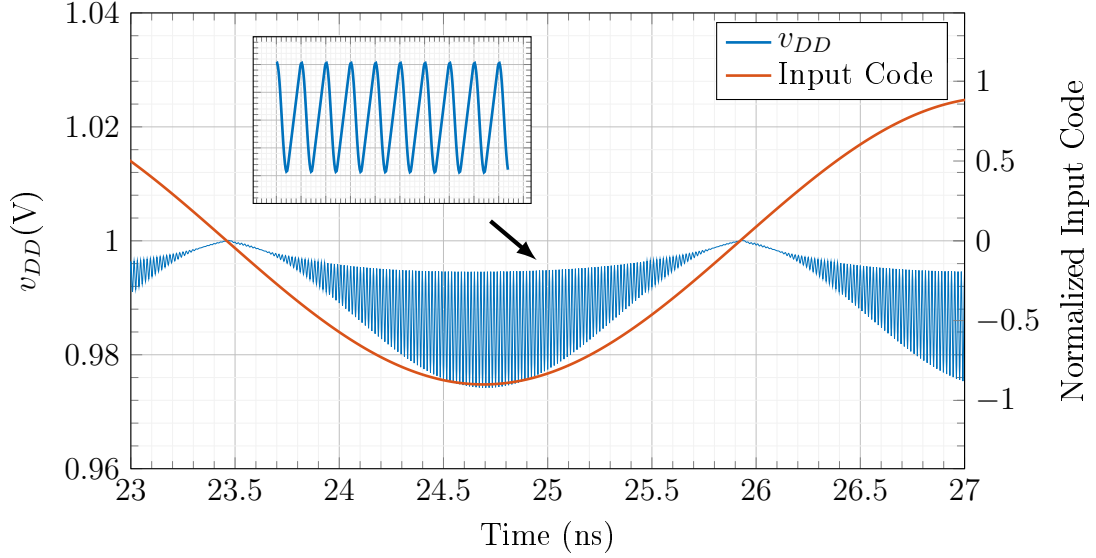
Figure 3.22: Simulated supply voltage variation including a supply network for a sinusoidal signal.

3.5 Discussion

This chapter presented a method to model a capacitive RF-DAC with switched linear and switched nonlinear state-space models, respectively. Switched LSSMs for the quadrature and the polar capacitive RF-DAC architectures are described, which are then extended to switched NSSMs. By considering the nonlinear relation of the effective on-resistance of the CMOS transistors to the drain-source voltage $|V_{ds}|$, the NSSM approach accounts for higher-order AM-PM effects. The comparisons with SpectreRF® simulations and measurement results show an excellent match of the switched NSSM in contrast to behavioral modeling approaches. The implemented model allows significantly shorter simulation run times compared to transistor-level SpectreRF® time-domain simulations. The switched nonlinear state-space modeling approach is a reliable way to mathematically describe and simulate capacitive RF-DACs with numerical simulators, providing superior accuracy and low simulation run times. However, simulation step size for polar architectures must be adopted according to the required accuracy of the phase modulation on the LO signal, i. e. rise/fall edges change with the baseband input signal's phase.

Furthermore, extensions to the switched state-space approach for capacitive RF-DAC modeling, covering crucial non-idealities such as capacitor mismatch, supply voltage variations, and LO phase noise were discussed. All of these impairments can be included in the model while maintaining the original benefits of low computational effort and low simulation run times, especially when comparing to circuit-level simulators. Furthermore, the dominant sources for spectral impairments can easily be identified. All effects can be introduced simultaneously or separately, allowing to detect the individual contributions.
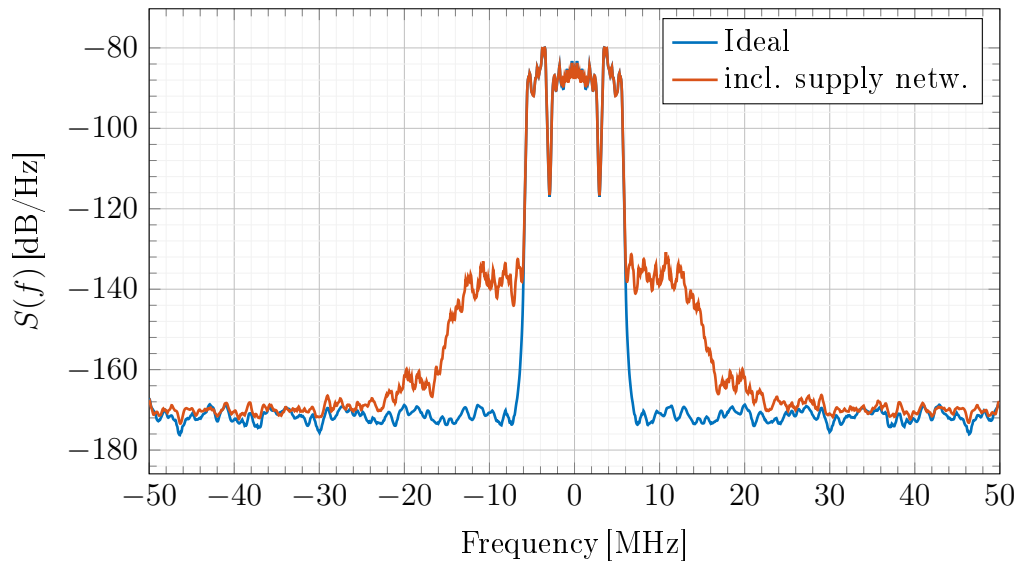
Figure 3.23: PSD of the downconverted RF-DAC output including a supply network for a multi-tone input signal with 10 MHz bandwidth.

The presented model allows for an efficient evaluation of RF-DAC impairments on concept-level and system-level. Furthermore, dominant sources of spectral degradation can quickly be assessed, also providing a powerful tool and quick insights for circuit designers.

The switched linear state-space model was first presented to the circuit and systems community [110]. The extension to the nonlinear approach resulted in a journal article [41]. Furthermore, an additional conference publication resulted, showing the possibilities of modeling the non-idealities of the RF-DACs [111]. Moreover, the modeling concept of the switched linear state-space models has also been applied to a high-speed current-steering DAC architecture [112].
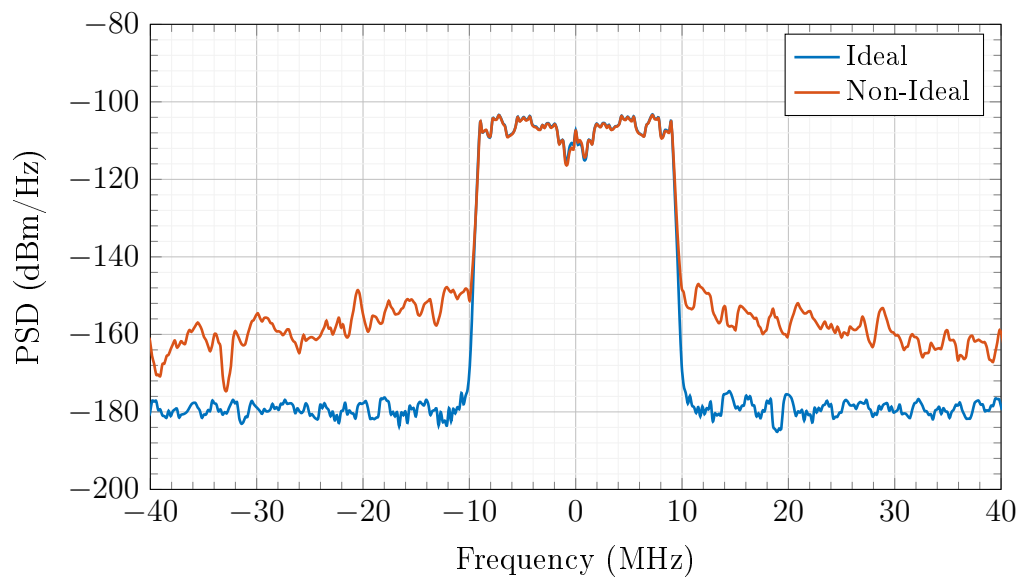
Figure 3.24: PSD of the RF-DAC output including all discussed impairments.

4 Supply Network Digital Predistortion for Capacitive RF DACs

This chapter presents details on the measures taken in the digital domain to compensate nonlinear distortions caused by supply voltage variations of capacitive RF-DACs. The developed concepts make use of digital predistortion techniques to suppress the effects caused by supply voltage distortions on the output of the RF-DAC, including a correction algorithm for voltage ripples from DC-DC converters and a circuit-inspired DPD approach to compensate the dynamic supply voltage variations caused by the nonideal supply network of the RF-DAC.

The capacitive RF-DAC combines high linearity over a wide frequency range with high power efficiency. The drawback of the design is its low power supply rejection. As a consequence, any distortions and noise affecting the supply translate to a degradation of its output signal.

Typically, low-dropout regulators (LDOs) are used to guarantee a stable supply voltage for capacitive RF-DACs. LDOs with a gain-bandwidth equal or larger the input signal bandwidth are needed to provide the necessary low supply impedance. To also keep track of higher intermodulation distortions (third, fifth, and higher-order), which are caused by a signal-dependent voltage drop over the supply network, LDOs with even higher gain-bandwidth would be needed. Specifically designed LDOs are still feasible to meet the required quality of the power supply for the capacitive RF-DAC for 4G communication [4]. However, for future wireless standards, the limits of this remedy will be reached, due to the necessity for further improvements in power efficiency and reduction in off-chip external components. Moreover, at the same time larger effective transmission bandwidths, 160 MHz and beyond, as well as higher constellation orders, exceeding 1024-QAM, will impose even more stringent quality requirements on the linearity and the dynamics of the capacitive RF-DAC. Furthermore, LDOs also suppress (deterministic) distortions of the supply such as voltage ripples from switching DC-DC converters.

The introduced digital ripple correction (DRC) concept uses a measured and time synchronized digital recreation of the actual DC-DC voltage ripple to modulate the input signal such that the distortion effect on the output signal of the RF-DAC is canceled.

The circuit-inspired digital predistortion technique compensates nonlinear effects introduced by the nonideal supply network of capacitive RF-DACs. The DPD concept recreates the signal-dependent voltage distortions of the capacitive

RF-DAC supply and utilizes this information to modulate the input signal such that the distortions on the output signal are canceled. The algorithm maps the RF-DAC input signal to an equivalent supply current and uses a digitally implemented supply network model to recreate the voltage distortion of the supply, which is then used to modulate the input signal. Its hardware demand is remarkably low compared to conventional (pruned) Volterra based solutions. The parametrization of the predistorter can be estimated by employing linear (low-complexity) adaptive system identification techniques. The presented concept is validated by measurements using a capacitive RF-DAC based digital power amplifier [5] and a wideband quadrature capacitive RF-DAC, similar to [6]. The proposed DPD approach, which is specialized for the supply network problematic outperforms conventionally used models such as the memory polynomial and the generalized memory polynomial. Throughout this thesis, the introduced concept is referred to as supply network digital predistortion (SNDPD).

Both concepts allow to either reduce the stringent requirements of the supply network and maintain the linearity of the overall system, or keep the specifications of the supply network and even increase the (linearity) performance of the RF-DAC.

4.1 Supply Voltage Variation of the Capacitive RF-DAC

The supply voltage V_{DD} of the capacitive RF-DAC is also its reference voltage. Hence, noise and distortions of the supply voltage are directly modulated with the input signal and the LO, causing undesired spectral regrowth and degradation of the in-band performance, as briefly sketched in Figure 4.1.

Apart from thermal noise, supply voltage variations are composed deterministic and random effects, including, but not limited to switching ripples of DC-DC converters [108]. However, the supply current $i_{DD}(t)$ drawn by the capacitive RF-DAC, is (input) signal dependent and is considered to be a random process due to the dependency on the input signal. The effects for both kinds of distortions are addressed in this section. Dedicated DPD concepts are discussed in Section 4.2 and Section 4.3, respectively.

Assuming a voltage distortion $v_d(t)$ on the supply, i.e. $v_{DD}(t) = V_{DC} + v_d(t)$, the first harmonic of the output of the capacitive RF-DAC (2.6) becomes

$$v_{\text{DAC}}(t) = \frac{2}{\pi} \, v_{DD}(t) \, \frac{n(t)}{N} \sin(\omega_{\text{LO}}t) \tag{4.1a}$$

$$= \frac{2}{\pi} \, [V_{DC} + v_d(t)] \, \frac{n(t)}{N} \sin(\omega_{\text{LO}}t) \,. \tag{4.1b}$$
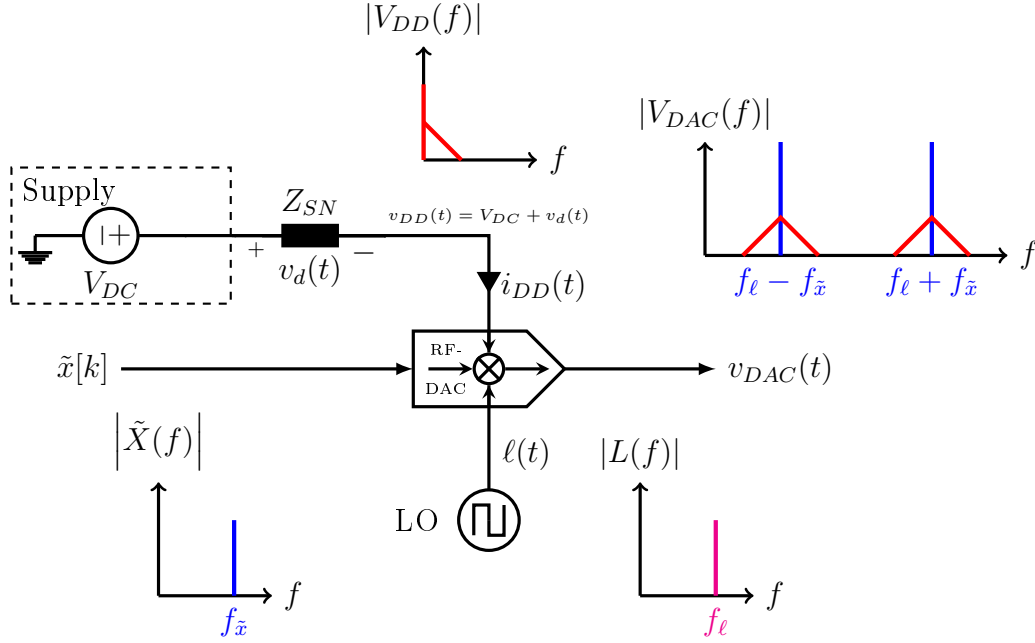
Figure 4.1: Effect of supply voltage variation on the output of the capacitive RF-DAC.

4.1.1 DC-DC Voltage Ripples

Switched DC-DC voltage regulators such as Buck converters generate switching harmonics, which are typically referred to as switching ripples $v_r(t)$ [91]. These are superimposed on the ideal supply voltage, i.e. $v_{DD}(t) = V_{DC} + v_r(t)$, generating undesired distortions in the output signal, as indicated in (4.1b). The impact of these DC-DC voltage ripples on the capacitive RF-DAC's output is shown in Figure 4.2 for a 10 mV peak-to-peak voltage ripple with 2 MHz fundamental switching frequency. The distortion caused by $v_r(t)$ significantly increases the ACPR in the near out-of-band region. Typically, these switching ripples are suppressed by on-chip LDOs. However, Section 4.2 presents a digital predistortion concept to suppress these distortions by modulating the input signal appropriately.

4.1.2 Signal Dependent Voltage Drop

The supply current $i_{DD}(t)$ drawn by the capacitive RF-DAC is (input) signal dependent, causing an undesired voltage drop $v_d(t)$ over the supply network impedance $Z_{SN} \neq 0$. This voltage drop results in variations of the RF-DAC supply, i.e. $v_{DD}(t) = V_{DC} + v_d(t)$, which are then modulated on the capacitive RF-DAC's output, resulting in spectral regrowth and in-band distortions as indicated in (4.1b).

The supply current $i_{DD}(t)$ is only drawn if active switching cells are connected to the supply. Figure 4.3a shows an exemplary supply current for a single-ended polar capacitive RF-DAC, where the supply current is only flowing when the LO gate connects the capacitor array to $v_{DD}(t)$. Thus, $i_{DD}(t)$ contains high-frequency components at the LO carrier frequency f_{LO} and its harmonics. Contrary, in
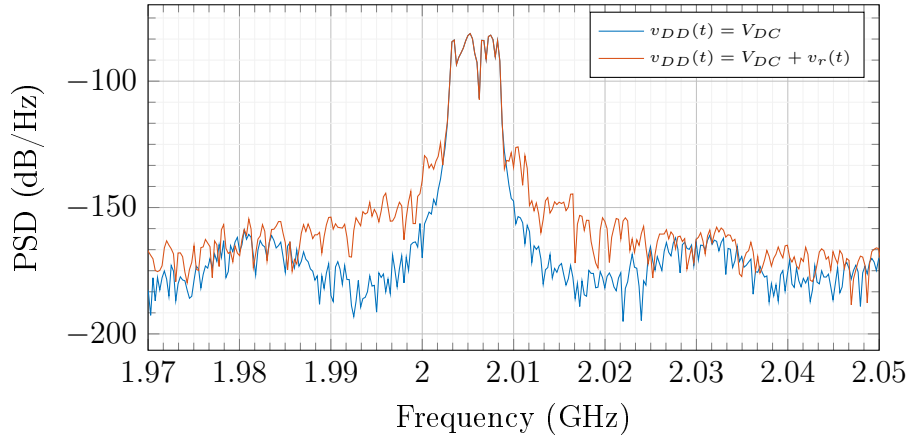
Figure 4.2: PSD of the capacitive RF-DAC output with and without a 10 mV peak-to-peak voltage ripple with 2 MHz fundamental switching frequency.

pseudo-differential designs active cells from either the P-side or the N-side are always connected to the supply [3–5, 30]. Hence, the input current is flowing at the high and low state of the LO, as shown in Figure 4.3b, thus shifting the high-frequency components to twice the LO carrier frequency. Due to imperfections parts remain at the fundamental LO carrier frequency, but are significantly reduced compared to the single-ended architecture.
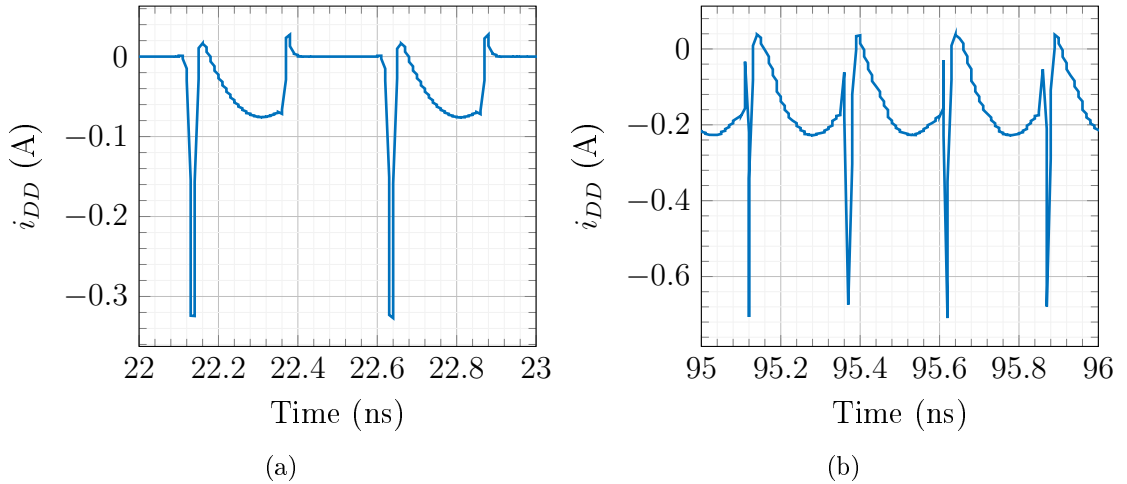

Figure 4.3: Input current waveforms of a polar capacitive RF-DAC with ideal supply network for (a) single-ended, and (b) pseudo-differential architecture, respectively.

Figure 4.3 shows the supply currents for a constant input signal, i. e. the number of active cells does not change. However, contrary to the constant capacitive RF-DAC's impedance (2.4) seen from the output, the impedance seen from the supply depends on the number of active switching cells. To show this, the RF-DAC is simplified to the model shown in Figure 4.4, similarly to the switched state-space approach above. All active and inactive cells are combined to two equivalent
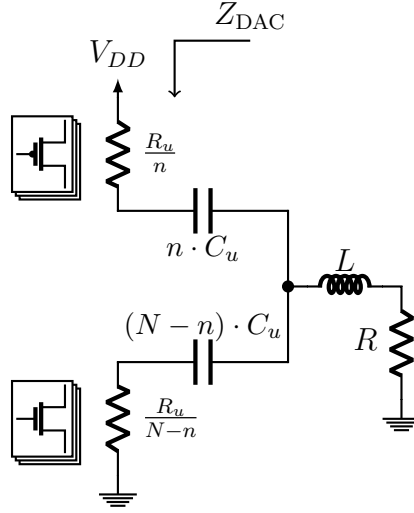
Figure 4.4: Simplified schematic model of the capacitive RF-DAC.

impedances, respectively. Without loss of generality C_u represents the (assumed) unitary capacitance of every cell, and R_u is the equivalent on-resistance of the drivers' PMOS and NMOS. The active cells are assumed to be connected to V_{DD}. With that, the input impedance of the RF-DAC is given by

$$Z_{\mathrm{DAC}}(s) = \frac{1}{n} \cdot \frac{s\,R_u\,C_u + 1}{s\,C_u} + \frac{(s\,R_u\,C_u + 1)\,(s\,L + R)}{(s\,R_u\,C_u + 1) + (N - n)\,s\,C_u\,(sL + R)}$$

$$= \frac{s\,R_u\,C_u + 1}{s\,C_u} \cdot \left[\frac{1}{n} + \frac{s\,L + R}{\frac{s\,R_u\,C_u + 1}{s\,C_u} + (N - n)\,(s\,L + R)} \right]. \tag{4.2}$$

Thus, the impedance changes with the baseband input signal $\tilde{x}[k]$. Figure 4.5 depicts the magnitude of $Z_{\mathrm{DAC}}(j\omega)$ evaluated at $\omega = \omega_{\mathrm{LO}}$.
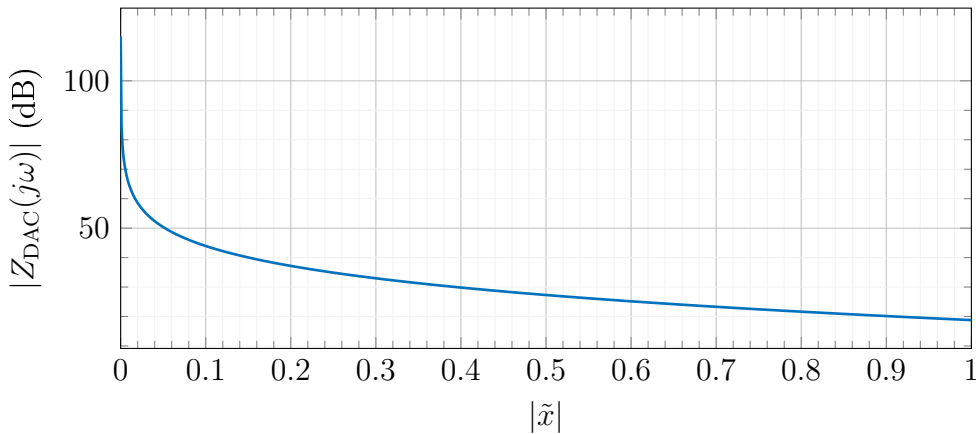

Figure 4.5: Magnitude of the input impedance $Z_{\mathrm{DAC}}(j\omega)$ of the capacitive RF-DAC over the normalized input signal.

The supply current, assuming an ideal supply voltage, is further given by

$$I_{DD}(s) = \frac{1}{Z_{\text{DAC}}(s)} V_{DC},$$

$$= V_{DC} \frac{s\,C_u}{s\,R_u\,C_u + 1} \frac{\frac{s\,R_u\,C_u+1}{s\,C_u} + (N-n)(sL+R)}{\frac{s\,R_u\,C_u+1}{s\,C_u} + (sL+R)N} \tag{4.3}$$

The resulting voltage drop over the supply network's impedance $Z_{\text{SN}}(s)$, assuming only linear components, is

$$V_d(s) = I_{DD}(s) \cdot Z_{\text{SN}}(s). \tag{4.4}$$

Henceforth, the supply current and consequently the voltage drop $v_d(t)$ are modulated by the input signal, resulting in low-frequency variations of $v_{DD}(t)$. These low-frequency voltage variations are then again modulated with the RF-DAC input signal and up-converted by the LO to the RF-DAC output, as mentioned above. Throughout the rest of this thesis, the term baseband distortions is used for the low-frequency variations, as these are correlated to the equivalent baseband input signal $\tilde{x}[k]$.

Similar to $i_{DD}(t)$ also $v_d(t)$ possesses high-frequency components at the LO frequency and its harmonics, respectively. The high-frequency distortions of $v_{DD}(t)$ at multiples of f_{LO} also contribute to the spectral regrowth at f_{LO} due to folding with harmonics of the rectangular (trapezoidal) LO signal. Nevertheless, these high-frequency variations are typically suppressed by the lowpass behavior of the supply network, minimizing their contribution to the RF-DAC output. Furthermore, suppression of the harmonics on the supply network can be improved by placing an additional blocking capacitor parallel to the RF-DAC. Consequently, for further analysis only the baseband distortions of $i_{DD}(t)$ and $v_{DD}(t)$ are investigated in detail. The high-frequency (switching) components, as depicted in Figure 4.3, are negligible and beyond the scope of DPD due to the required oversampling.

Average Supply Current

The drawn low-frequency supply current, i.e. the baseband distortions, can be approximated by applying the input signal to a static nonlinear function, which maps the equivalent number of active switching cells to an averaged input current $g : x_{\text{on}} \rightarrow \overline{i_{DD}}$, where $x_{\text{on}} = \frac{n}{N}$ represents the normalized number of active switching cells.

The relation of x_{on} to the input signal $\tilde{x}[k]$ differs for polar and quadrature architectures. In polar architectures, the number of active switching cells is determined by the magnitude of the input signal. Contrary, for quadrature capacitive RF-DACs it depends on the sum of the magnitudes of the in-phase and the quadrature signal. Hence, the normalized number of active switching cells for polar and quadrature architectures, respectively, is given by

$$x_{\text{on}}[k] = O_n(\tilde{x}[k]) = \begin{cases} |\tilde{x}[k]| & \text{for polar} \\ |x_I[k]| + |x_Q[k]| & \text{for quadrature} \end{cases} \tag{4.5}$$

where $\tilde{x}[k] = x_I[k] + j\,x_Q[k]$ and $n[k] \propto x_{\text{on}}[k]$. Henceforth, also the baseband distortions on $v_{DD}(t)$ depend either on the magnitude of the input signal or on the sum of the magnitudes of the in-phase and the quadrature input signal.

Nevertheless, the input current is only determined by the instantaneous number of active switching cells, and hence on the input signal. Thus $g(\cdot)$ is treated as an instantaneous nonlinearity, similar to the models discussed in Section 2.2.2, i.e. $\overline{i_{DD}}(t) = g\left[x_{\text{on}}(t)\right]$, where $\overline{i_{DD}}(t)$ represents the signal dependent low-frequency supply current. Due to the nonlinear relation, the bandwidth of the distortions on the supply is in general larger than the input signal's bandwidth, increasing also the bandwidth of the spectral leakage at the RF-DAC output.

The average supply current for each input code of the RF-DAC $\overline{i_{DD}}$ can be determined by applying a respective constant input code to the RF-DAC and perform a time averaging over the measured current drawn from the supply. Figure 4.6 shows the average supply current for a polar capacitive RF-DAC over the whole input signal range.
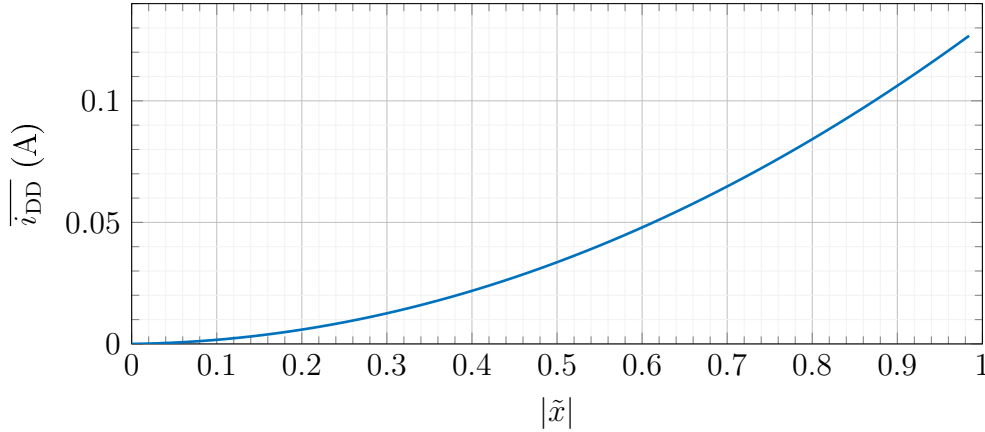

Figure 4.6: Average capacitive RF-DAC supply current over normalized input signal magnitude for a polar architecture.

Polar Capacitive RF-DAC Architectures

In polar architectures, the number of active cells depends on the magnitude of the input signal, i.e. $n \propto x_{\text{on}} = |\tilde{x}|$ as in (4.5). Hence, the input impedance Z_{DAC} is determined by the magnitude of the complex-valued input signal. Thus, the resulting drawn supply current depends on the magnitude of the input signal, i.e.

$$\overline{i_{DD}} = g\left(x_{\text{on}}\right) = g\left(|\tilde{x}|\right). \tag{4.6}$$

Consequently, also the voltage drop $v_d(t)$ depends on the magnitude of the input signal. The supply voltage of a polar architecture, for $V_{DC} = 1\,\text{V}$, is depicted in Figure 4.7. The voltage drop corresponds to the magnitude of the chosen real-valued input signal, i.e. $\tilde{x}[k] \in \mathbb{R}$ (no phase modulation of the LO). Independent

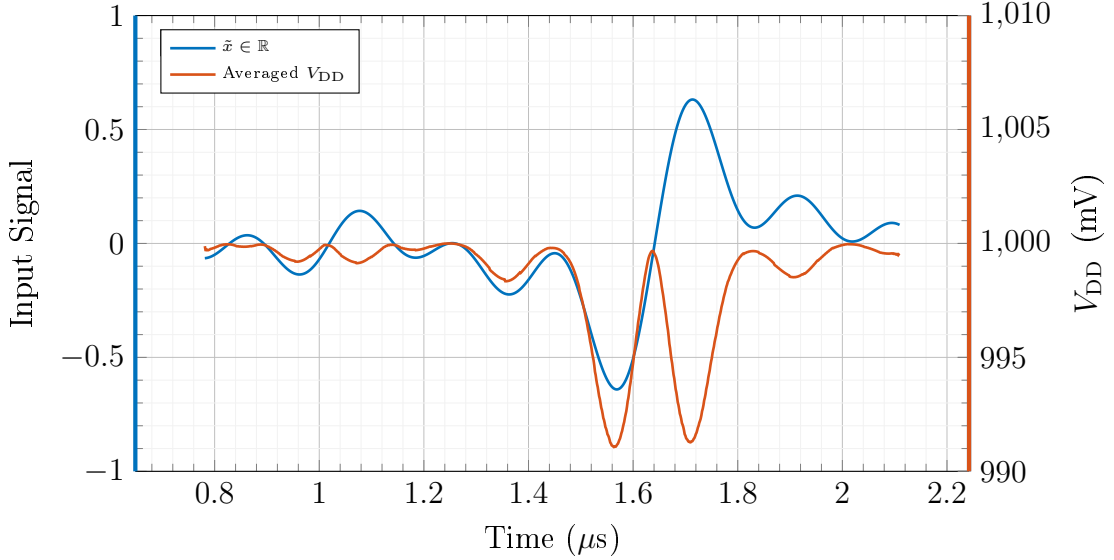of the sign of the input signal, the supply voltage $v_{DD}(t)$ is always lower than the ideal V_{DC}.

Figure 4.7: Variation of the supply voltage $v_{DD}(t)$ of a polar architecture for a real-valued input signal $\tilde{x}[k] \in \mathbb{R}$. $v_{DD}(t)$ drops proportionally to the magnitude of the input signal.

Figure 4.8a shows the PSD of $v_{DD}(t)$ of a polar capacitive RF-DAC, connected to a passive RLC supply network, using a 14 MHz real-valued (no phase modulation) sinusoidal input signal. Due to the absolute value in (4.6), the first harmonic of the distortion on $v_{DD}(t)$ appears at twice the input signal frequency, i.e. at 28 MHz. Figure 4.8b shows the PSD of an (ideal) polar capacitive RF-DAC with ideal and nonideal supply network, respectively. The distortion tones of the supply voltage, which start appearing at twice the input signal frequency, cause intermodulation products at $f_{\mathrm{LO}} \pm 3m\,f_{\mathrm{sig}}$ at the output of the RF-DAC.

As mentioned above, the input current of the capacitive RF-DAC can be simulated or measured using constant input signal levels. The resulting equivalent low-frequency input current for a given constant input signal is then calculated by averaging out the high-frequency switching current. Alternatively, the low-frequency baseband distortion of the supply current could also be approximated by the inverse of the capacitive RF-DAC input impedance (4.2), i.e.

$$\left|\overline{I_{DD}}(\mathrm{j}\omega)\right| = \frac{1}{|Z_{\mathrm{DAC}}(\mathrm{j}\omega)|}\,\frac{2}{\pi^2}, \tag{4.7}$$

where $\frac{2}{\pi^2}$ results from the average, rectified value and the absolute value of the fundamental tone of the square wave LO signal. However, (4.7) only holds if the active switching cells are connected to $v_{DD}(t)$ and only for one fixed number of switching cells n. Thus, (4.7) must be re-evaluated for each n.

Figure 4.9 shows the comparison of the approximation (4.7) to the simulated average supply current using the switched LSSM as described in Section 3.2.1.
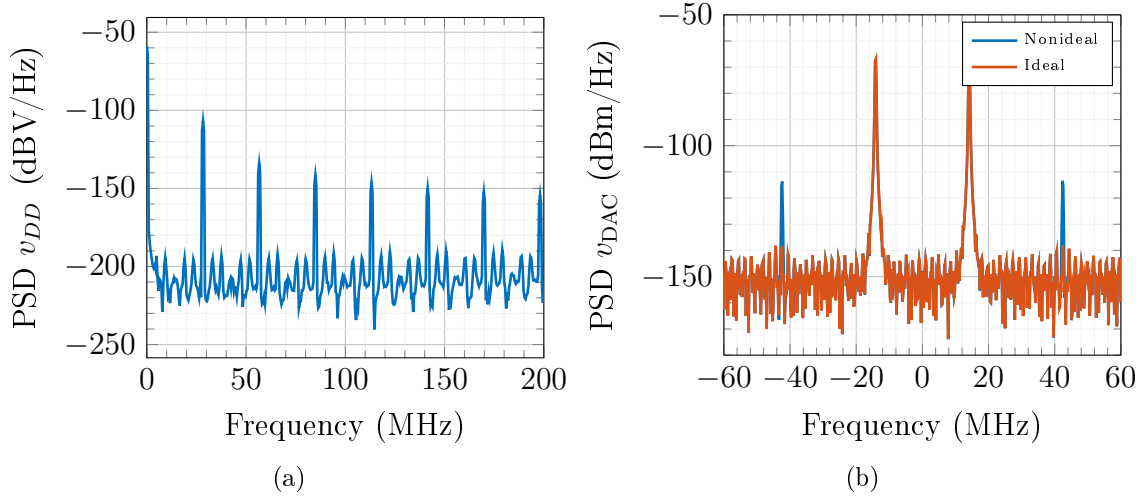
Figure 4.8: PSD of the supply voltage $v_{DD}(t)$ and the down-converted RF-DAC output signal of a polar architecture for a real-valued sinusoidal input signal.

Z_{DAC} is derived from the lumped model used in the switched LSSM to provide a fair comparison. The approximation of $\overline{i_{DD}}$ with (4.7) still yields a good match to the evaluated time-domain simulation. We note that Z_{DAC} is evaluated using the equivalent on-resistance of the PMOS devices $R_u = f(r_{\mathrm{pmos}})$, and thus for close-to-fullscale input signals, where almost only PMOS devices are switched, $\frac{1}{|Z_{\mathrm{DAC}}(j\,\omega_{\mathrm{LO}})|}$ yields a good approximation of $\overline{i_{DD}}$. However, for small input signal values, where only few PMOS devices are active, the approximation deviates from the actual current drawn by the RF-DAC, as indicated in logarithmic scale in Figure 4.9b. Thus the average current should either be derived from transistor-level simulations, from measurements or directly included in the estimation of the DPD model parameters. The latter approach is used in the proposed DPD.

Quadrature Capacitive RF-DAC Architecture

The active switching cells of the quadrature capacitive RF-DAC depend on the sum of the magnitudes of the in-phase and the quadrature signals as in (4.5), resulting in different effects compared to the polar architecture. Thus, also the input current is no longer a function of the input signal magnitude, but given by

$$\overline{i_{DD}}(t) = g\left(x_{\mathrm{on}}\right) = g\left[|x_I(t)| + |x_Q(t)|\right] \tag{4.8}$$

Typically, the in-phase and the quadrature cells are connected to the same supply. A simplified schematic is shown in Figure 4.10, where again a unitary cell
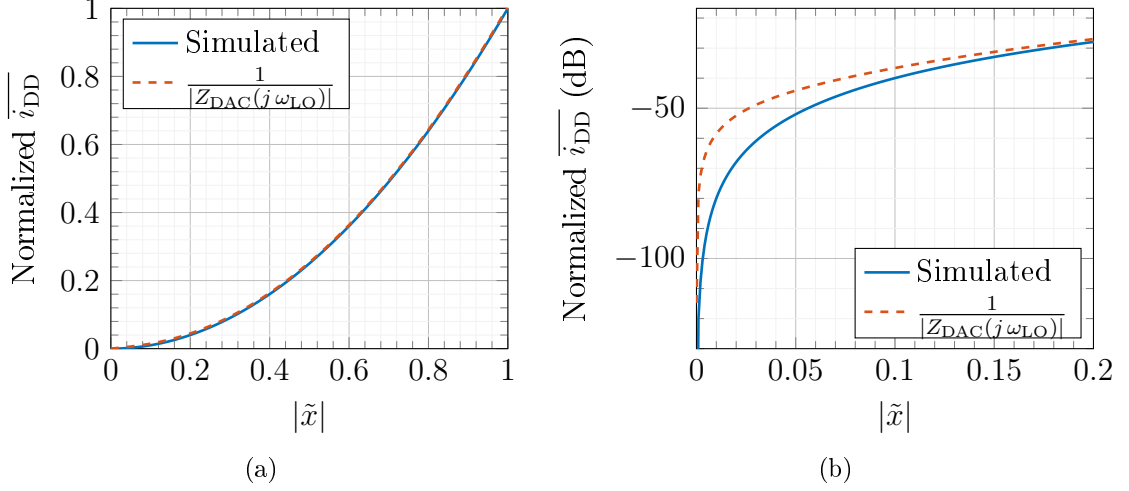
Figure 4.9: Comparison of the simulated (switched LSSM) and the approximated average input current of a polar capacitive RF-DAC for (a) the full input signal range, and (b) only for low input signal levels.

design is assumed with

$$r_{I_{\mathrm{on}}} = \frac{R_u}{n_I}, \qquad\qquad c_{I_{\mathrm{on}}} = C_u \cdot n_I, \qquad\qquad (4.9\mathrm{a})$$

$$r_{Q_{\mathrm{on}}} = \frac{R_u}{n_Q}, \qquad\qquad c_{Q_{\mathrm{on}}} = C_u \cdot n_Q, \qquad\qquad (4.9\mathrm{b})$$

$$r_{\mathrm{off}} = \frac{R_u}{N - n_I - n_Q}, \qquad\qquad c_{\mathrm{off}} = C_u \cdot (N - n_I - n_Q). \qquad (4.9\mathrm{c})$$

The equivalent number of active cells, as mentioned above, depends on the sum of the in-phase and quadrature input signal magnitudes, i.e.

$$n \propto |x_I(t)| + |x_Q(t)|, \qquad\qquad (4.10\mathrm{a})$$
$$N - n \propto 1 - |x_I(t)| - |x_Q(t)|. \qquad\qquad (4.10\mathrm{b})$$

Figure 4.11 shows the normalized average supply current $\overline{i_{DD}}$ over the in-phase and the quadrature input signal levels for the model shown in Figure 4.10. The resulting supply current is thus a two-dimensional function, depending on the assumed independent in-phase and quadrature component of the input signal.

As a result, also the baseband distortions $v_d(t)$ on $v_{DD}(t)$ depend on the sum of magnitudes of the in-phase and quadrature input signal. Figure 4.12 shows the supply voltage drop, for $V_{DC} = 1.1\,\mathrm{V}$, for a quadrature capacitive RF-DAC. The sudden changes of the supply voltage of the quadrature architecture correspond to the discontinuities of $|x_I| + |x_Q|$. In contrast, at the same time instances, the magnitude $|x_I + jx_Q|$ is smooth. Furthermore, these discontinuities excite the resonance behavior of the RLC supply network and cause the ringing on $v_{DD}(t)$, as can be seen in Figure 4.12.
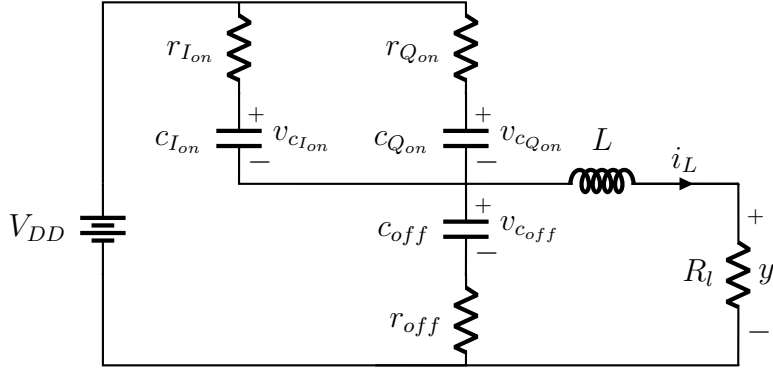
Figure 4.10: Equivalent circuit for a quadrature capacitive RF-DAC when both, I and Q related cells are connected to V_{DD}.
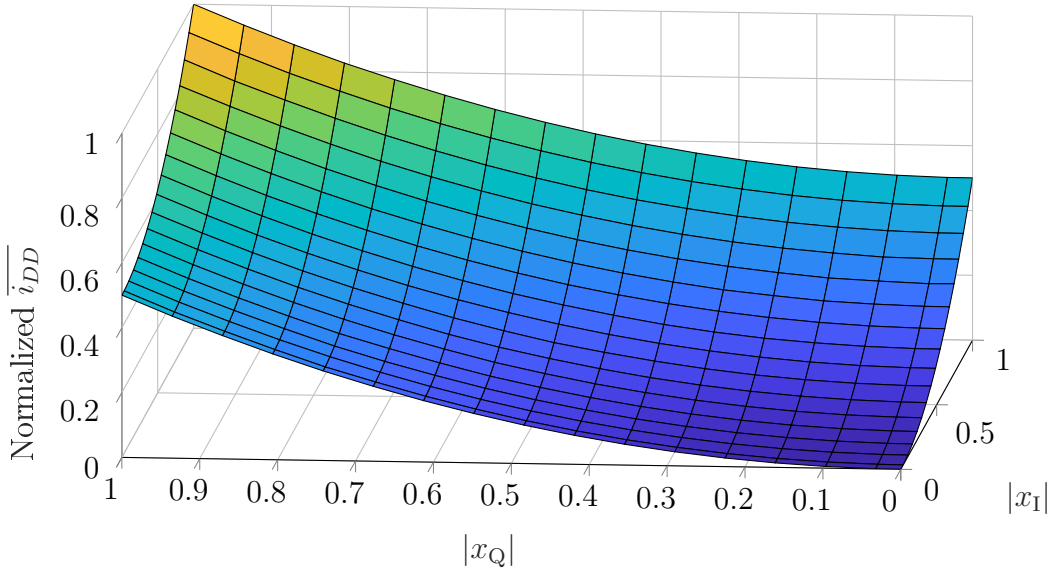
Figure 4.11: Normalized $\overline{i_{DD}}$ over in-phase and quadrature signal magnitudes.

The dependency of $v_d(t)$ on the sum of magnitudes also increases the bandwidth of the distortions, even compared to the polar case. Figure 4.13a shows the PSD of $v_{DD}(t)$ of a quadrature capacitive RF-DAC, connected to a passive RLC supply network, using a 14 MHz complex-valued sinusoidal input signal, i. e. $x(t) = \cos(2\pi f_{\text{sig}} t) + j \sin(2\pi f_{\text{sig}} t)$. Contrary to the polar architecture, the first distortion tone on $v_{DD}(t)$ is at four times the frequency of the input signal, i. e. at 56 MHz. In polar architectures, the voltage drop over V_{DD} results in a DC offset as the magnitude and hence the number of switching cells is constant. Figure 4.13b shows the respective output spectrum of the quadrature capacitive RF-DAC with ideal and nonideal supply network.

Additionally, the supply network also causes IQ crosstalk for quadrature architectures if in-phase and quadrature cells are connected to the same supply. Assuming the model of the RF-DAC in (4.1b) and a complex-valued input signal

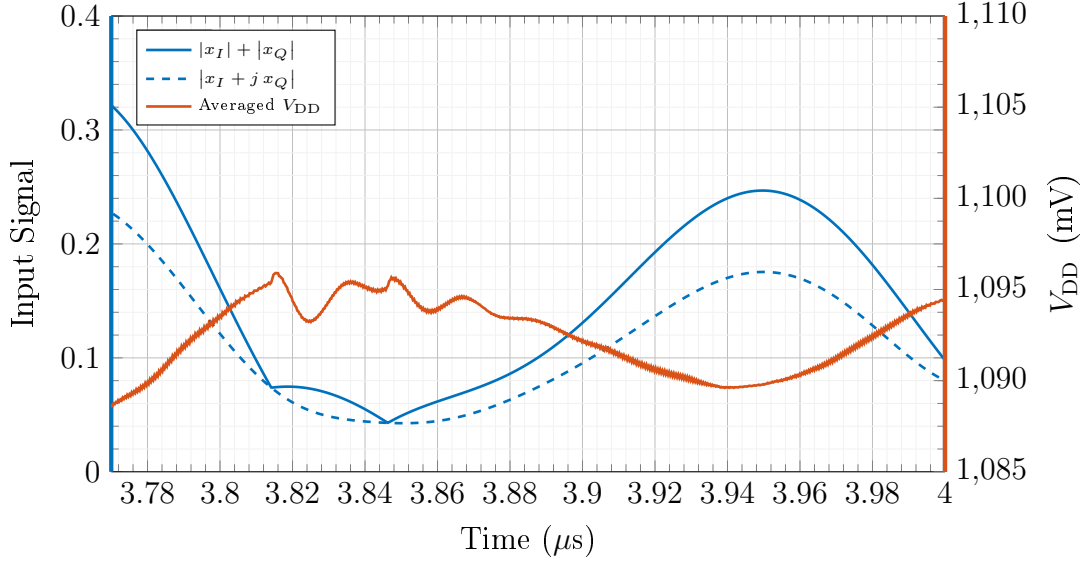Figure 4.12: Variation of the supply voltage $v_{DD}(t)$ of a quadrature capacitive RF-DAC. The sudden changes of the supply voltage correspond to the discontinuities of $(|x_I| + |x_Q|)$.

$\tilde{x}(t) = x_I(t) + j\, x_Q(t)$, the output of the capacitive RF-DAC becomes

$$
\begin{aligned}
v_{\mathrm{DAC}}(t) &= \frac{2\, v_{DD}(t)}{\pi}\ [x_I(t)\, \cos(\omega_{\mathrm{LO}}t) - x_Q(t)\, \sin(\omega_{\mathrm{LO}}t)] \\
&= \frac{2}{\pi}\ [V_{DC} + v_d(t)]\ [x_I(t)\, \cos(\omega_{\mathrm{LO}}t) - x_Q(t)\, \sin(\omega_{\mathrm{LO}}t)] \\
&= x_I(t)\, \cos(\omega_{\mathrm{LO}}t)\, \frac{2}{\pi}\ [V_{DC} + v_d(t)] - x_Q(t)\, \sin(\omega_{\mathrm{LO}}t)\, \frac{2}{\pi}\ [V_{DC} + v_d(t)].
\end{aligned}
\tag{4.11}
$$

Due to the nonlinear relation of the supply current on the sum of magnitudes (4.8), also the supply voltage variation depends on the the in-phase and quadrature input signals, i. e.

$$
v_d(t) = G\left\{|x_I(t)| + |x_Q(t)|\right\}.
\tag{4.12}
$$

Putting this into (4.11) yields

$$
\begin{aligned}
v_{\mathrm{DAC}}(t) = {}& x_I(t)\, \cos(\omega_{\mathrm{LO}}t)\, \frac{2}{\pi}\ [V_{DC} + G\left\{|x_I(t)| + |x_Q(t)|\right\}] \\
& - x_Q(t)\, \sin(\omega_{\mathrm{LO}}t)\, \frac{2}{\pi}\ [V_{DC} + G\left\{|x_I(t)| + |x_Q(t)|\right\}],
\end{aligned}
\tag{4.13}
$$

showing that the in-phase and quadrature signal components are each modulated by the supply voltage distortion, which depends on both $x_I(t)$ and $x_Q(t)$. Henceforth, the supply network also causes IQ crosstalk in quadrature RF-DAC architectures.

Similar as for the polar architecture, the average input current could be approximated by using the equivalent input impedance Z_{DAC}. One approach is to
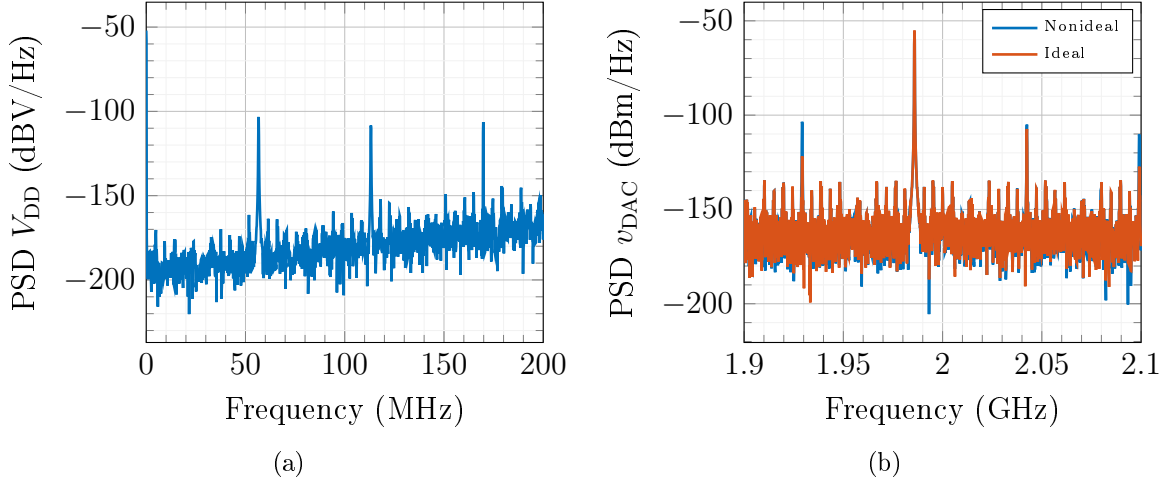
Figure 4.13: PSDs of the supply voltage $v_{DD}(t)$ and the corresponding output of the capacitive RF-DAC in (a) and (b), respectively.

transform the circuit model shown in Figure 4.10 to the same form as the polar architecture in (4.2) but with component values as in (4.9). However, this neglects the fact that the in-phase and quadrature LO signals possess a 90° phase shift. Due to this, there are four resulting phases where the active in-phase and quadrature cells are connected to V_{DD}, respectively, i. e.

$$\text{LO}_\text{I} = 1, \text{LO}_\text{Q} = 0$$
$$\text{LO}_\text{I} = 0, \text{LO}_\text{Q} = 0$$
$$\text{LO}_\text{I} = 0, \text{LO}_\text{Q} = 1$$
$$\text{LO}_\text{I} = 1, \text{LO}_\text{Q} = 1$$

Assuming an additive (linear) behavior of the resulting circuits of the respective LO switching states, the total average input current can be approximated by the superposition of all individual circuit structures. This is further referred to as four-phase model. The resulting approximated average input current is then given by

$$\overline{I_{DD}}(\mathrm{j}\omega) = \frac{1}{2\pi} \sum_{i=0}^{1} \sum_{j=0}^{1} \left\{ \frac{1}{Z_{\text{DAC}_{\text{LO}_\text{I}=i, \text{LO}_\text{Q}=j}} (\omega_\text{LO} t)} \right\} \qquad (4.14)$$

for i, j defining the individual LO signal states.

The approach using the equivalent polar circuit and the four-phase approach are compared to the evaluated average current using again the switched LSSM approach. Figure 4.14 shows the relative error of the approximations (4.2) and (4.14). The equivalent polar model, using $x_\text{on} = |x_I| + |x_Q|$ fails in predicting the average input current for $\Phi_{c(t)} = m\frac{\pi}{4}$, i. e. maximum x_I, minimum x_Q, and vice versa. The four-phase model, on the other hand, shows a very good match for $\Phi_{c(t)} = m\frac{\pi}{4}$, but lacks accuracy in the diagonal, i. e. $\Phi_{c(t)} = m\frac{\pi}{8}$ for $m = 1, 3, 5, \ldots$.

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Conclusively, neither of the investigated quasi-linear approximations results in a valid method to predict the average input current. Henceforth, estimating the input current is integrated in the parameter estimation of the proposed DPD approach in Section 4.3.
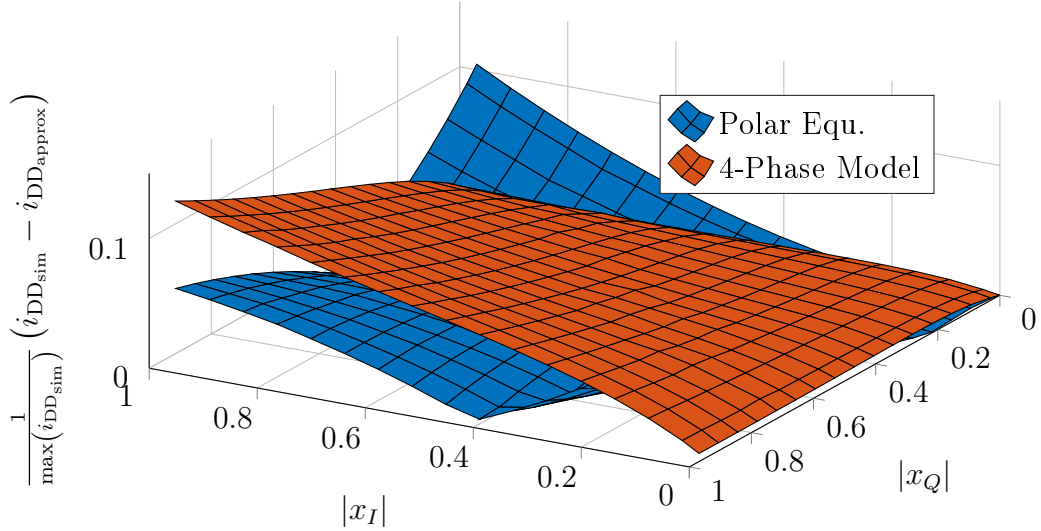

Figure 4.14: Error between the approximated input current and the simulated input current for the polar equivalent (4.7) and the four-phase superposition approach (4.14).

4.2 Digital Compensation of DC-DC Converter Voltage Ripples

As already mentioned in Section 4.1.1, switched DC-DC voltage converters introduce voltage distortions on v_{DD}. These so-called voltage ripples $v_r(t)$ are independent of the dynamic load changes of the RF-DAC caused by the input code. Typically, less complex LDOs are required for just suppressing $v_r(t)$ due to the relatively slow switching frequency of the DC-DC converter. Nevertheless, by exploiting the deterministic behavior of the switching ripple, the introduced distortions can also be canceled by digital signal processing techniques, circumventing the need for a dedicated LDO.

The proposed concept modulates the RF-DAC input signal $\tilde{x}[k]$ such that the distortions caused by supply voltage variation are canceled at the output. The proposed predistortion function is given by

$$\tilde{u}[k] = \tilde{x}[k] \frac{1}{\left(1 + \frac{v_r[k]}{V_{DC}}\right)}, \tag{4.15}$$

where $\tilde{u}[k]$ is the predistorted input signal of the capacitive RF-DAC, and $v_r[k]$ is the digital representative of the DC-DC converter's voltage ripple [108]. Inserting (4.15) into the ideal input-output function of a polar capacitive RF-DAC (4.1b)

yields an ideal compensation of the voltage ripple:

$$
\begin{aligned}
v_{\text{DAC}}(t) &= \frac{2}{\pi} \left[V_{DC} + v_r(t) \right] |\tilde{u}(t)| \sin\left(\omega_{\text{LO}} t + \varphi(t)\right) \\
&= \frac{2}{\pi} \sin\left(\omega_{\text{LO}} t + \varphi(t)\right) \left[V_{DC} + v_r(t) \right] |\tilde{x}(t)| \frac{1}{\left(1 + \frac{v_r(t)}{V_{DC}}\right)} \\
&= \frac{2}{\pi} \sin\left(\omega_{\text{LO}} t + \varphi(t)\right) \left[V_{DC} + v_r(t) \right] |\tilde{x}(t)| \frac{V_{DC}}{(V_{DC} + v_r(t))} \\
&= \frac{2}{\pi} \sin\left(\omega_{\text{LO}} t + \varphi(t)\right) V_{DC} |\tilde{x}(t)|
\end{aligned}
\tag{4.16}
$$

where $\tilde{x}(t) = |\tilde{x}(t)| e^{i \varphi(t)}$ and $\tilde{u}(t)$ are the continuous-time representations of the digital input signals, respectively. Similar derivation can be applied to the quadrature capacitive RF-DAC architecture.

Unfortunately, (4.16) requires knowledge of $v_r[k]$, which is typically not available. Therefore, the voltage ripple must either be approximated by estimating the supply network or measured with an additional ADC. This section discusses the use of a dedicated ADC for compensating the deterministic DC-DC voltage ripple. The supply network estimation concept is discussed in Sec. 4.3. Estimation of the DC-DC converter filter circuitry may be achieved by using its internal feedback ADC, if available. However, the DC-DC converter is typically an external device with no access to its internals. Consequently, the proposed approach uses a dedicated ADC to measure the voltage ripple.

The ADC, on the other hand, is limited by its resolution and has a finite conversion time, reducing the achievable suppression by the predistortion approach. Furthermore, the required changes of the input signal in (4.15) are typically in the range of a few LSBs of the capacitive RF-DAC as $|v_r(t)| \ll V_{DC}$ [91]. Thus, even with a perfect ADC, the highest achievable compensation of voltage ripples with (4.15) is limited by the resolution of the capacitive RF-DAC itself. The achievable suppression can be approximated by[1] [108]

$$
\Gamma_{\text{dB}} \approx 6.02 \left[\log_2 \left(\frac{|\tilde{x}|}{V_{DC}} v_{r_{pp}} \right) \cdot B \right] + 1.76,
\tag{4.17}
$$

where $v_{r_{\text{pp}}}$ is the peak-to-peak amplitude of the switching ripple $v_r(t)$ and $|\tilde{x}|$ is the input signal magnitude with $0 \le |\tilde{x}| \le 1$, both assumed to be sinusoidal signals, respectively. B is the number of bits of the capacitive RF-DAC. Henceforth, the achievable compensation for a Nyquist ADC is limited by the resolution of the capacitive RF-DAC, the peak-to-peak amplitude of the voltage ripple $v_{r_{pp}}$, and the input signal magnitude $|\tilde{x}|$. Furthermore, from (4.17) the maximum required resolution of the ADC to omit additional quantization noise can be deduced. There is no benefit in using a higher resolution. Figure 4.15 shows the analytical approximation of (4.17) and simulation results for the suppression Γ_{dB} with constant input signal $|\tilde{x}| \in [0.01, 1]$.

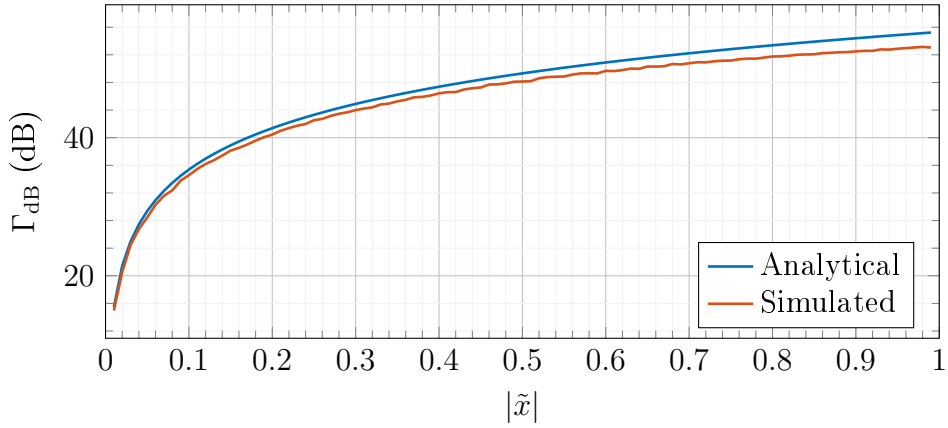[1]Similar to the commonly SNR evaluation for ADCs.

Figure 4.15: Analytical approximation (4.17) and simulated ripple suppression Γ_{dB} over the normalized input signal magnitude $|\tilde{x}|$.

Moreover, also the required sampling frequency and the conversion time of the ADC must be considered. The ADC's sampling frequency has to be chosen according to the Nyquist-Shannon criterion such that it is at least twice the practically relevant bandwidth of the voltage ripple. Due to the switching behavior of the DC-DC converter, the voltage ripples may possess discontinuities, hence increasing the bandwidth of $v_r(t)$. This must be considered when choosing the sampling frequency. Nevertheless, due to the DC-DC output network, which typically forms a lowpass filter, higher harmonics are suppressed and do not affect practical implementations. Hence, sampling rates in the range of ten times the DC-DC converter's switching frequency have shown to be sufficient.

However, the finite conversion time of the ADC imposes a significant problem as it introduces a timing mismatch between the measured digital ripple $v_r[k]$ and the actual voltage ripple on the supply $v_r(t)$ of the capacitive RF-DAC. Furthermore, an additional delay is caused by the implementation of the digital algorithm (4.15). This results in significant performance degradation of the proposed cancellation concept. Figure 4.16 shows the achievable suppression Γ_{dB} of the voltage ripple at the output of the capacitive RF-DAC for different time mismatches Δt of the digital ripple $v_r(kT_S - \Delta t)$ with respect to the analog ripple $v_r(t)$. A delay of only $10\,\mathrm{ns}$ for a $1\,\mathrm{MHz}$ voltage ripple already results in a drop of the ripple suppression of more than $30\,\mathrm{dB}$.

Flash converter ADCs with high clock rates may reduce the conversion time but drastically increase the required current consumption. Similarly, also the delay caused by the digital implementation of the predistortion algorithm can be reduced with higher clock rates. However, this limits the efficiency in terms of power consumption for implementations. In the following, an enhanced method to overcome the delay problem in the DPD approach is presented.

The DC-DC converter is assumed to operate in a steady-state with a fixed switching frequency to guarantee a stable output voltage. Hence, the voltage ripple is periodic with the DC-DC switching frequency, i.e. $v_r(t) = v_r(t + m\,t_{\mathrm{DC-DC}})$,
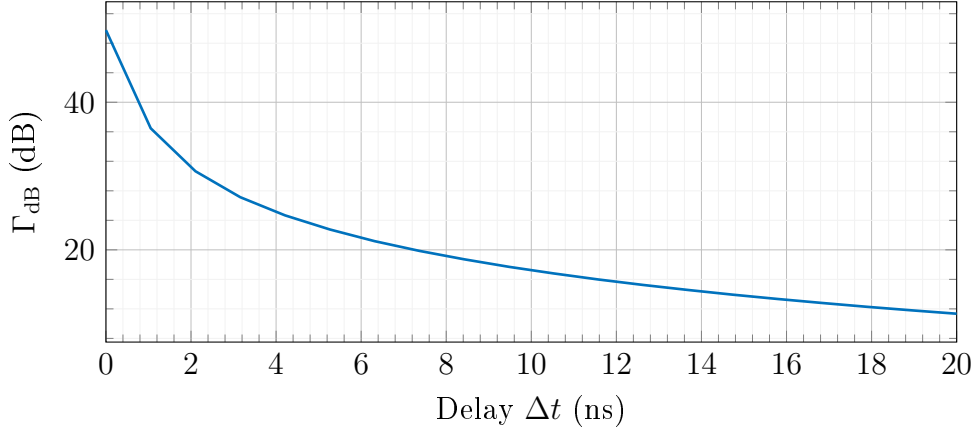
Figure 4.16: Suppression Γ_{dB} for increasing delay of the digital ripple $v_r(kT_S - \Delta t)$ for a 1 MHz DC-DC converter switching voltage ripple.

where $t_{\mathrm{DC-DC}} = \frac{1}{f_{\mathrm{DC-DC}}}$. Utilizing this property, the measured ripple $v_r[k]$ is intentionally delayed to the next switching period of the DC-DC converter such that the shifted and the actual voltage ripple overlap. The digital ripple $v_r[k]$ must therefore be delayed by the DC-DC converter's switching period $t_{\mathrm{DC-DC}}$ minus the conversion delay Δt_{ADC} of the ADC, and the delay Δt_{DPD} caused by the digital processing of the algorithm (4.15), i. e.

$$t_{\mathrm{shift}} = t_{\mathrm{DC-DC}} - \underbrace{(\Delta t_{\mathrm{ADC}} + \Delta t_{\mathrm{DPD}})}_{\Delta t}. \tag{4.18}$$

Hence, the error $e_{\Delta t}$ introduced by the improper timing can be eliminated as depicted in Figure 4.17.
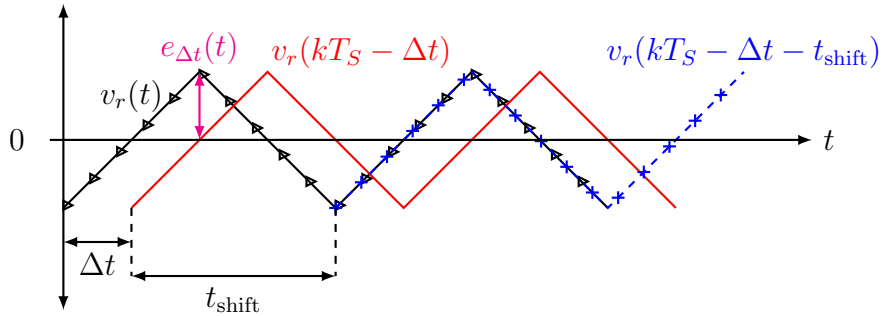
Figure 4.17: Delay of the digital ripple $v_r[k]$ to the next DC-DC switching period.

The structure of the proposed approach with an additional delay element t_{shift} and an optional memory is presented in Figure 4.18, where the delay of the ADC t_{ADC} and the DPD t_{DPD} are already combined to Δt after the ADC. Integer ratios of the clock signals of the ADC, the DC-DC converter, and the DFE allow using simple shift registers as $\frac{t_{\mathrm{shift}}}{T_{\mathrm{s}}}$ is also an integer. In general, fractional delays can also be used, but increase the complexity. A precise shifting can be achieved by

synchronizing the phases of the respective clock signals, where $f_{\text{DC-DC}} \ll f_{\text{ADC}} \leq f_{\text{DFE}}$, respectively. As a result, the specifications for the conversion time of the ADC can be significantly relaxed. This enables using power efficient converters such as successive approximation (SAR) ADCs. Furthermore, small area and low power digital architectures for (4.15), e.g. pipeline structures, can be used.

Optionally, one period of the measured voltage ripple can be stored in a separate memory as indicated in Figure 4.18. The stored ripple can then be used in the digital algorithm with proper timing. Hence, the ADC can be switched off, further decreasing the power consumption of the total transmitter. To compensate for time variations and imperfections in the DC-DC converter, the stored voltage ripple can be re-measured by periodically activating the ADC.
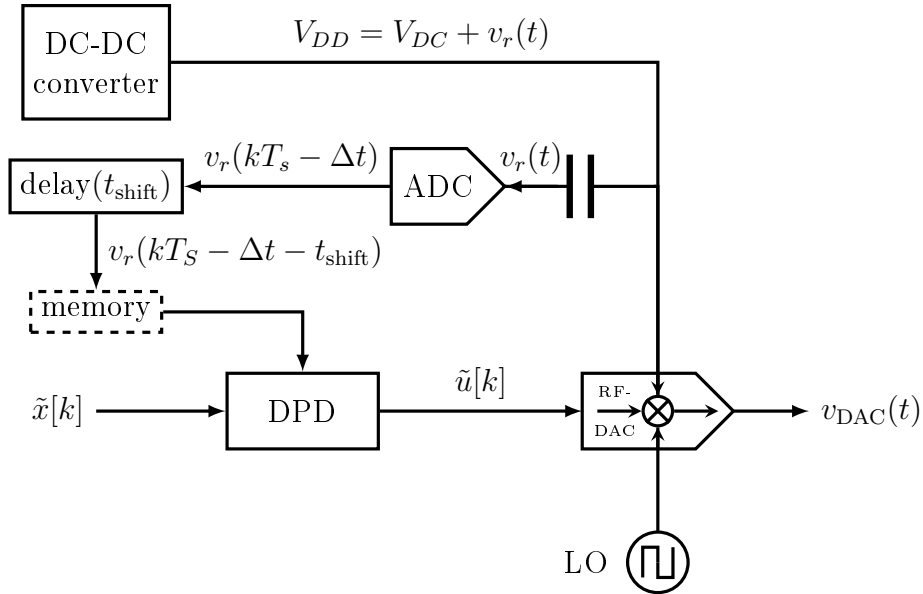
Figure 4.18: Block diagram of the DC-DC converter voltage ripple compensation approach using an intended delay of the measured voltage ripple for the predistortion function.

Figure 4.19 shows the simulation results of the digital compensation approach for a single-tone signal and a multi-tone signal, respectively. Simulations are performed with MATLAB/Simulink, where the capacitive RF-DAC is realized with the LSSM as described in Section 3.2.1. The state-space matrices are given in Appendix B.1. The DC-DC converter (buck converter) is modeled by separate switched state-space model [91] and its output voltage waveform is used as input $u(t)$ for the LSSM of the RF-DAC. The ADC is assumed to be ideal, except for a finite resolution and a fixed conversion time Δt_{ADC}. The clock frequencies are set to 2 GHz for the LO, 200 MHz for the DFE, 40 MHz for the ADC, and 2 MHz for the DC-DC converter. The clock signals of the DC-DC converter, the DFE, and the ADC are phase-aligned. For both, single-tone and multi-tone signals, the DPD with a timing mismatch of $t_0 = t_{\text{shift}} + 10\,\text{ns}$ between actual voltage ripple $v_r(t)$ and the delayed digital ripple shows only minor suppression of the out-of-band distortions. However, a precise shift, i.e. $t_0 = t_{\text{shift}}$, as suggested in (4.18)

results in a significant reduction of the ripple distortions with the proposed digital compensation technique.
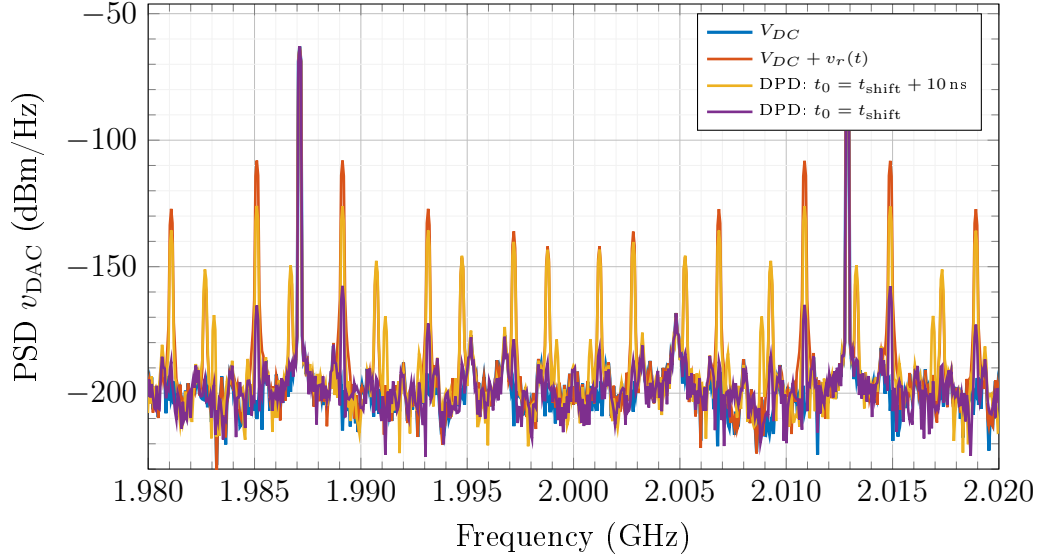
(a)
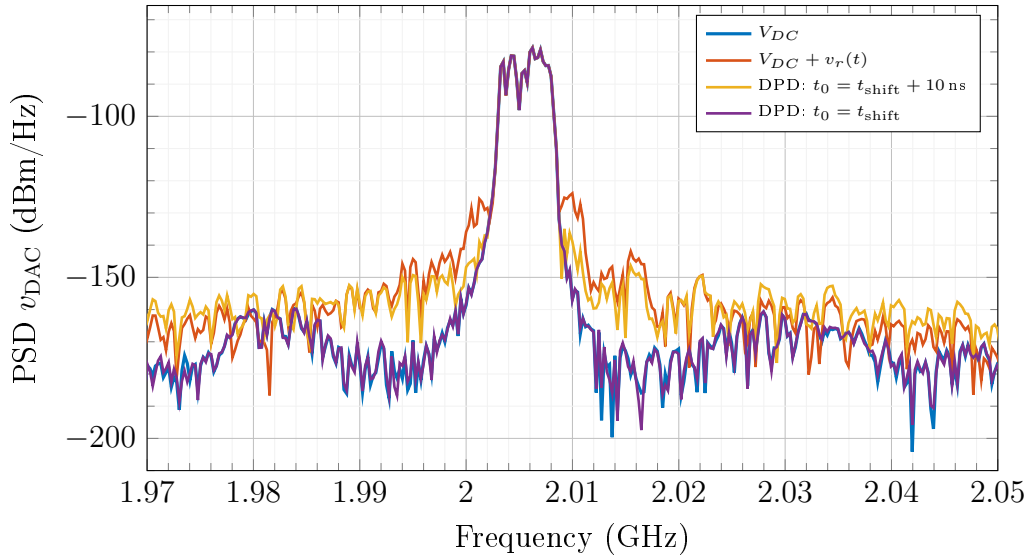
(b)

Figure 4.19: Compensation of DC-DC converter voltage ripples for (a) a single-tone signal and (b) a multi-tone signal.

4.2.1 Drawback of the Ripple Correction Algorithm

The proposed approach to compensate DC-DC converter voltage ripples is limited by the assumption of the steady-state condition of the DC-DC converter. In practice, the measured voltage ripples $v_r[k]$ are only approximately periodic but

in two consecutive switching periods the change of the voltage ripples is marginal. Henceforth, the delay to the next period is a valid approach to compensate the periodic ripple $v_r(t)$ and reduce the requirements or even omit the LDO.

Nevertheless, the total supply voltage distortions additionally change dependent on the RF-DAC input signal as described in Section 4.1.2. Simulations as shown in Figure 4.19 show the potential of the digital ripple correction approach. However, these simulations use two distinct state-space models, and the feedback current of the RF-DAC is not modeled here. Further investigations using transistor level simulations showed that the effect of a current feedback must not be omitted, otherwise only the (assumed) periodic ripples are corrected.

The effect of the signal dependent voltage variations $v_d(t)$ on the RF-DAC output is similar to the DC-DC converter voltage ripples $v_r(t)$. Thus, an ideal cancellation of the voltage variations could be achieved by applying the ripple correction predistortion in (4.15). Nevertheless, this method requires a priori knowledge of $v_d(t)$ and an accurate timing. Furthermore, an additional ADC is required to continuously measure the actual voltage distortion. For periodic signals such as the DC-DC voltage ripple, the shifting method can be used. However, this technique is unfeasible for the signal dependent voltage drop as the input signal is typically random data. Thus it cannot be predicted nor assumed to be periodic. The conversion delay and the required sampling rate of the ADC render this DPD approach unfeasible for the signal dependent distortions. Moreover, a possible estimation of $v_d[k]$ with (4.15) requires a nonlinear estimator, as is discussed below.

Nevertheless, one could try and estimate the signal dependent voltage distortion $v_d[k]$ and utilize this to modulate the input code with (4.15). Using a memory polynomial approach for the estimation of $\hat{v}_d[k]$ yields

$$\hat{v}_d[k] = \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm}\, \tilde{x}[k-m]\, |\tilde{x}[k-m]|^{j-1}\,, \tag{4.19}$$

. The predistorted input signal is thus given by

$$\tilde{u}[k] = \tilde{x}[k]\, \frac{V_{DC}}{\left(V_{DC} + \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm}\, \tilde{x}[k-m]\, |\tilde{x}[k-m]|^{j-1}\right)}. \tag{4.20}$$

Inserting this into an idealized baseband model of the RF-DAC transfer characteristic, i.e. $\tilde{v}_{\mathrm{DAC}}[k] = \tilde{u}[k]\, (V_{DC} + v_d[k])$ gives

$$\tilde{v}_{\mathrm{DAC}}[k] = \tilde{x}[k]\, \frac{V_{DC}}{\left(V_{DC} + \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm}\, \tilde{x}[k-m]\, |\tilde{x}[k-m]|^{j-1}\right)}, \tag{4.21}$$

which shows that the parameters a_{jm} are nonlinear in the output $\tilde{v}_{\mathrm{DAC}}[k]$. Henceforth, nonlinear estimation algorithms are required, resulting in high complexity for the estimator, which increases the required power and area for the DPD. Furthermore, the robustness and stability of the nonlinear estimation approach must also be considered.

To conclude, the proposed delay and predistortion technique provides a good solution to compensate the effects of DC-DC converter voltage ripples on the output signal but can't be used to mitigate the effects of the signal dependent voltage drop over the supply network. Another compensation technique for the signal dependent voltage variation of the supply voltage is discussed in the next section.

4.3 Circuit-Inspired Digital Predistortion

The proposed digital predistortion concept is based on the analysis of the supply network effects discussed in Section 4.1, focusing on the suppression of the code dependent voltage variations $v_d(t)$ due to an imperfect supply network.

This section solely focuses on the equivalent (digital) baseband signal. Thus, all signals and functions are represented as discrete-time samples, i.e. $x(t) \rightarrow x(k \cdot T_s) = x[k] \in \mathbb{C}$. Furthermore, also the tilde symbol for the equivalent baseband signals is omitted. Consequently, the ideal capacitive RF-DAC input-output characteristic from (2.6) is reduced to

$$v_{DAC}[k] = v_{DD}[k] \cdot x[k] = x[k] \cdot (V_{DC} + v_d[k]), \qquad (4.22)$$

where $x[k]$ is the equivalent baseband input signal and $v_d[k]$ represents the baseband (low-frequency) distortions of the supply voltage, as discussed above. $v_{DAC}[k]$ is the equivalent baseband output signal of the RF-DAC, where (2.6) assumes a zonal filter at the RF-DAC's output. Furthermore, the constant factor $\frac{2}{\pi}$ is omitted here.

DC-DC voltage ripple effects can be overcome by LDOs with a bandwidth in the few MHz range, or by the concept presented before. However, the dominant frequency components of the code dependent voltage drop possess a much higher bandwidth as discussed in Section 4.1.2. Furthermore, with increasing signal bandwidth for future radio communications standards such as Wi-Fi 802.11ax and 5G, the design of dedicated LDOs will soon reach its limit[2]. Therefore, digital predistortion offers an efficient method to cancel supply voltage variations while maintaining the same requirements for the LDO.

The overview of the proposed circuit inspired DPD concept is briefly sketched in Figure 4.20. The DPD re-creates the voltage drop over Z_{SN} in the digital domain and modulates the input signal such that the effects of the varying supply voltage on the output of the RF-DAC are suppressed.

The proposed predistortion algorithm uses a modified Hammerstein predistorter concept to estimate the voltage distortion $v_d[k]$ based on the input signal and the measured capacitive RF-DAC output signal. Furthermore, the developed approach allows to use linear low complexity estimation concepts.

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[2]Still considering a moderate current consumption.
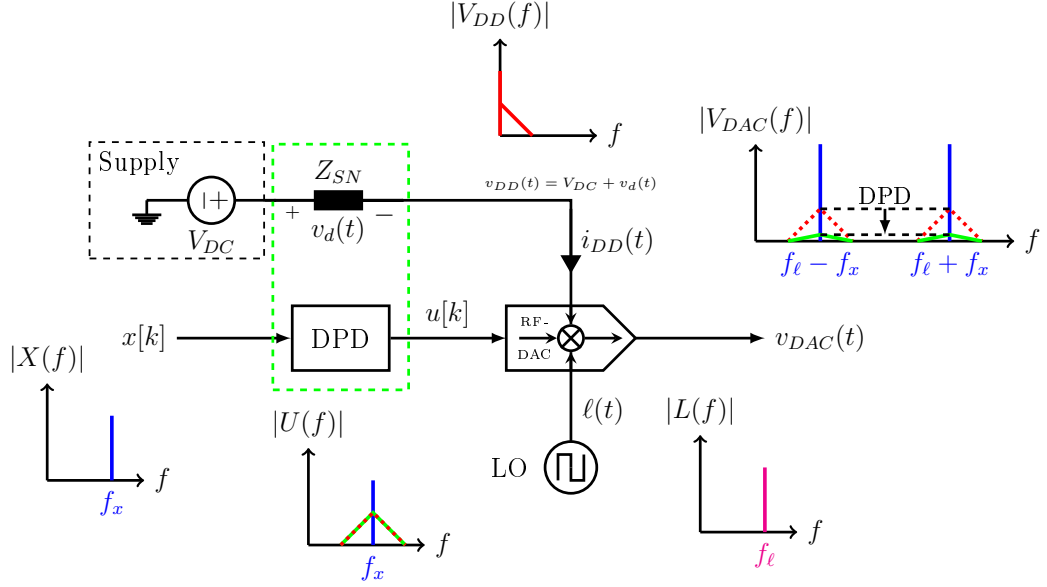
Figure 4.20: The circuit inspired supply network DPD concept modulates the input signal with an estimated voltage drop such that the effects of a varying supply voltage on the output of the capacitive RF-DAC are suppressed.

4.3.1 Motivation of the Proposed Concept

To achieve suppression of the supply voltage distortion $x[k]$ is modulated by a signal $\alpha[k]$ such that the predistorted RF-DAC input signal $u[k]$ is given by

$$u[k] = x[k] \cdot (1 - \alpha[k]) . \tag{4.23}$$

Inserting (4.23) into the ideal RF-DAC transfer characteristic (4.22) yields

$$
\begin{aligned}
v_{DAC}[k] &= u[k]\, v_{DD}[k] \\
&= \{x[k]\, (1 - \alpha[k])\}\, v_{DD}[k] \\
&= x[k]\, (1 - \alpha[k])\, [(V_{DC} + v_d[k])] \\
&= x[k]\, [V_{DC} + v_d[k] - \alpha[k]\, V_{DC} - \alpha[k]\, v_d[k]]
\end{aligned}
\tag{4.24}
$$

Hence, an ideal compensation of $v_d[k]$ would be achieved by

$$\alpha[k] = \frac{v_d[k]}{V_{DC}} \left(\frac{1}{1 + \frac{v_d[k]}{V_{DC}}} \right) . \tag{4.25}$$

However, the signal dependent voltage distortions $v_d[k]$ are unknown, and are, as described above, dominated by the parasitic supply network components of the RF-DAC. Thus $\alpha[k]$ is infeasible to be accurately predicted by simulation and is therefore targeted to be estimated. Furthermore, choosing $\alpha[k]$ as in (4.25) results in a nonlinear parameter estimation problem as discussed in Section 4.2.1.

Therefore, assuming $v_d[k] \ll V_{DC}$ and thus $\frac{v_d[k]}{V_{DC}} \ll 1$, $\alpha[k]$ can be approximated by

$$\alpha[k] = \frac{v_d[k]}{V_{DC}}, \tag{4.26}$$

which leads to the RF-DAC output signal

$$v_{DAC}[k] = x[k] \cdot \left(V_{DC} - \frac{v_d[k]}{V_{DC}} \cdot v_d[k] \right). \tag{4.27}$$

The term $x[k] \cdot \left(\frac{v_d[k]}{V_{DC}} \cdot v_d[k] \right)$ represents a systematic error introduced by the DPD (4.23) caused by the proposed approximation of $\alpha[k]$ in (4.26). However, $(v_d^2[k])$ is almost at the RF-DAC's (quantization) noise floor level. For example, taking an 8 mV drop of $v_{DD}(t)$ from Figure 4.7 and referring it to a 15 bit RF-DAC with a 1 V reference voltage results in approximately 2 LSBs of the RF-DAC for $v_d^2[k]$. Hence, the contribution of $x[k] \cdot \left(\frac{v_d^2[k]}{V_{DC}} \right)$ is negligible, such that

$$v_{DAC}[k] = x[k] \cdot \left[V_{DC} - \underbrace{v_d[k] \cdot \alpha[k]}_{\approx 0} \right]$$

$$\approx x[k] \cdot V_{DC} \tag{4.28}$$

yields the desired, distortion free output.

The concept (4.23) with $\alpha[k]$ as proposed in (4.26) does not represent a perfect inversion of the RF-DAC's nonlinearity. However, the dominating distortions caused by $v_d[k]$ can be canceled as indicated in (4.28). Furthermore, choosing $\alpha[k]$ as in (4.26) allows to use linear estimation algorithms similar to conventionally used DPD approaches as will be described below.

4.3.2 Concept of the DPD

The details of the proposed DPD are shown in Figure 4.21, which was filed with the US patent office and granted in 2018 [113]. The algorithm maps the RF-DAC input signal $x[k]$ to an equivalent supply current and uses a digitally implemented supply network model to recreate the voltage distortion $\hat{\alpha}[k] = \frac{\hat{v}_d[k]}{V_{DC}}$, which is further used as a modulation signal for the input signal. The hat symbol indicates that $\hat{\alpha}[k]$ and hence $\hat{v}_d[k]$ are now considered to be estimates of the actual voltage distortion as $v_d[k]$ is unknown a priori. The concept is valid for polar and for quadrature capacitive RF-DAC designs.

The block with $O_n\left(x[k]\right)$ in Figure 4.21 maps the input signal to the normalized number of active switching cells $x_{\text{on}}[k]$, depending on the RF-DAC architecture as in (4.5).

$g\left(x_{\text{on}}\right)$ is a static nonlinear function, mapping the equivalent number of active cells $x_{\text{on}}[k]$ to the low-frequency input current $i_{DD}[k]$ of the capacitive RF-DAC. This function is comparable to an instantaneous nonlinearity used in Wiener and
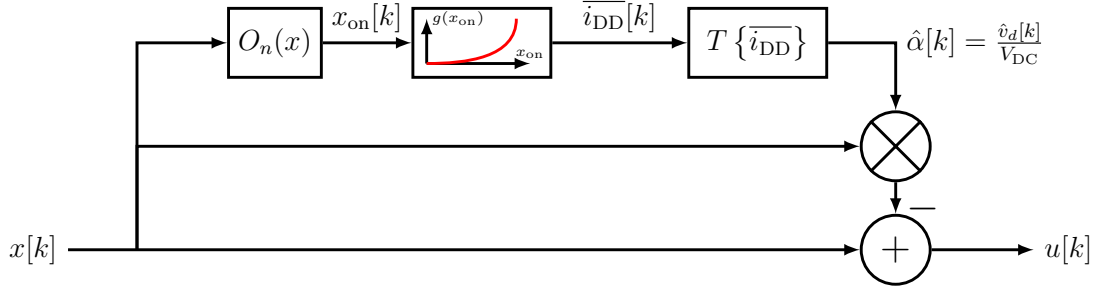
Figure 4.21: Concept of supply network predistortion [113].

Hammerstein models [25,26]. For example, $g(x_{on})$ can be modeled by a polynomial with order J or by a lookup table, where the respective coefficients are determined either by measurements or by circuit level simulations. Figure 4.22 shows a second-order polynomial, modeling the simulated low-frequency supply current of a polar capacitive RF-DAC for constant input signal magnitudes.
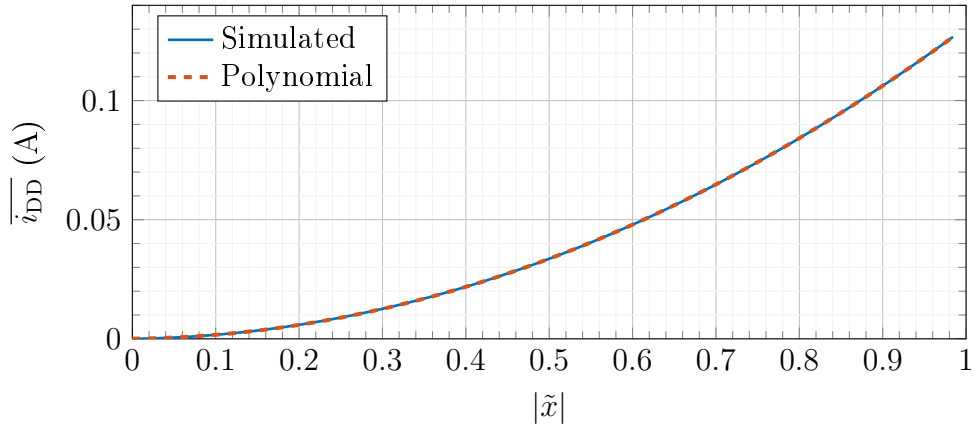
Figure 4.22: Average capacitive RF-DAC supply current over normalized input signal magnitude for a polar-based architecture.

Finally, the operator $T\{\cdot\}$ models the frequency dependent supply network impedance as indicated in (4.4). The output $\hat{\alpha}[k]$ of $T\{\cdot\}$ is an estimate of the actual voltage drop $v_d[k]$ over the supply network, normalized by V_{DC}. The supply network characteristic are dominated by parasitic effects due to wiring and process variation. Therefore, predicting its values with simulation is unreliable for DPD and hence $\hat{\alpha}[k]$ is targeted to be estimated. In contrast to the static nonlinear function $g(x_{on})$ the model of the supply network $T\{\cdot\}$ accounts for frequency dependent effects of the supply network, including inductive and capacitive effects. Thus, the proposed approach incorporates compensation of static nonlinearities as well as dynamic (memory) effects.

The output of the supply network model $\hat{\alpha}[k]$ is first multiplied with $x[k]$ and then subtracted from the input signal $x[k]$. The resulting mathematical represen-

tation of the concept is given by

$$y[k] = x[k] \cdot (1 - \hat{\alpha}[k]) \tag{4.29a}$$

$$= x[k] \cdot \left(1 - \frac{\hat{v}_d[k]}{V_{DC}}\right) \tag{4.29b}$$

$$= x[k] \cdot (1 - T\left\{g\left(x_{\mathrm{on}}[k]\right)\right\}) . \tag{4.29c}$$

4.3.3 Modified Parallel Hammerstein Model

To be implemented, the static and dynamic nonlinearities in (4.29c) must be realized with mathematical functions. In this work, $g(x_{\mathrm{on}})$ is modeled by a polynomial of order J. The operator $T\left\{\cdot\right\}$ is realized by a digital FIR filter of length M, which models the impulse response of the supply network as indicated in (4.4), i.e. $T\left\{\cdot\right\} \to T[k] = \sum_{m=0}^{M-1} h_m\, \delta[k - m]$. Thus $\hat{\alpha}[k]$ is given by

$$\hat{\alpha}[k] = \sum_{m=0}^{M-1} h_m \cdot \left(\sum_{j=0}^{J} g_j \cdot x_{\mathrm{on}}^j[k - m]\right), \tag{4.30}$$

having $(J + 1 + M)$ coefficients. Inserting $\hat{\alpha}[k]$ in the proposed DPD (4.23) gives

$$y[k] = x[k] \cdot \left[1 - \sum_{m=0}^{M-1} h_m \cdot \left(\sum_{j=0}^{J} g_j \cdot x_{\mathrm{on}}^j[k - m]\right)\right] . \tag{4.31}$$

Using (4.30) to model the voltage distortion is similar to a typically used Hammerstein approach, where a static nonlinear function is followed by one FIR filter. Moving h_m inside the inner sum and introducing the new coefficients $a_{jm} = h_m \cdot g_j, \forall\, (m = 0, \dots, M - 1\,, j = 0, \dots, J)$ leads to

$$u[k] = x[k] \left(1 - \sum_{m=0}^{M-1} \sum_{j=0}^{J} a_{jm}\, x_{\mathrm{on}}^j[k - m]\right), \tag{4.32}$$

with the signal model given by

$$\hat{\alpha}[k] = \frac{\hat{v}_d[k]}{V_{DC}} = \sum_{m=0}^{M-1} \sum_{j=0}^{J} a_{jm}\, x_{\mathrm{on}}^j[k - m]. \tag{4.33}$$

Considering the a_{jm} as $(J + 1) \cdot M$ independent coefficients leads to an even more general DPD concept, where separate FIR filters are applied for each monomial as depicted in the block diagram in Figure 4.23. Furthermore, with (4.32) the output is linear in the parameters a_{jm} and linear estimation algorithms can be used as will be shown below.

The derived DPD (4.32) uses a parallel filter structure similar to the general (parallel) Hammerstein model [71] and the MP. Furthermore, the SNDPD shows

similarities to the envelope memory polynomial model (EMP) [74, 114]. However, the input to the SNDPD's predistorter depends on the normalized number of switching cells $x_{\mathrm{on}}[k]$, changing with the architecture of the RF-DAC as in (4.5). Although, for polar architectures where $x_{\mathrm{on}}[k] = |x[k]|$ the proposed SNDPD is equivalent to the EMP (2.68) as shown in Appendix A.3.
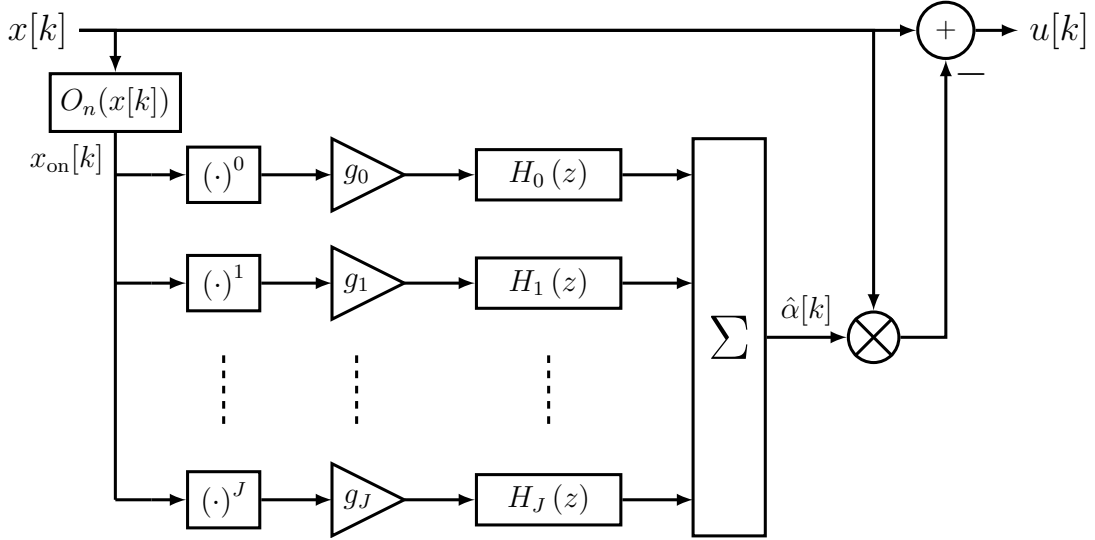

Figure 4.23: Block diagram of the proposed SNDPD for polar and quadrature capacitive RF-DAC architectures.

Implementation Complexity

The SNDPD model's block diagram for polar and quadrature architectures is shown in Figure 4.23. The difference between the polar and the quadrature solution as shown in Figure 4.23 is only the input to the nonlinear parallel filter structure.

The proposed DPD structure has similarities to the memory polynomial sketched in Figure 4.24. Similar to the derived approach, also the MP consists of parallel FIR filter structures, as shown in Figure 4.24. However, the parallel filter structure of the MP requires the complex-valued equivalent baseband signal as input. This results in complex multiplications within each filter stage. Furthermore, the baseband input signal also needs to be delayed and multiplied in each FIR stage as given in (2.66b), hence requiring additional delay elements in the implementation.

In a straight forward implementation, i. e. no specific optimization for multiplications, the memory polynomial requires in total 90 real-valued multiplications and 26 real-valued additions for a polynomial of order $J = 3$ and $M = 5$ memory taps for each FIR filter $H_j(z)$. For the same coefficient set, i. e. $J = 3$ and $M = 5$, the SNDPD requires only 34 real-valued multiplications and 29 real-valued additions. The multiplications of the distinct power terms $|\cdot|^j$ have been neglected from this analysis, as they are equal for both approaches. However, the complexity of the SNDPD is very similar to the EMP.
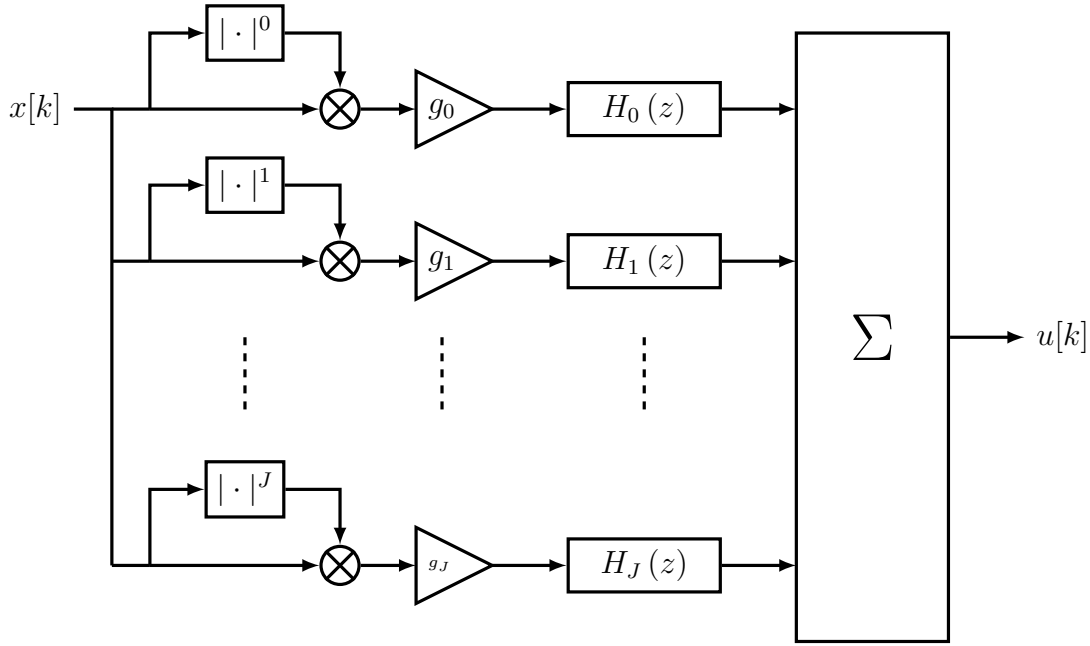
Figure 4.24: Block diagram of the Memory Polynomial.

4.3.4 Parameter Estimation

The goal is to estimate the parameters a_{jm} through observation of the equivalent baseband output signal $v_{DAC}[k]$ of the RF-DAC, similar to typically used DPD models such as the MP and the GMP. With (4.22) and using vector notation, the RF-DAC output without DPD can be rewritten as

$$v_{\text{DAC}}[k] = x[k] \left(V_{DC} + \underbrace{\mathbf{x}_{\text{on}}[k]^T \mathbf{a}_{jm}}_{\hat{\alpha}[k]} \right), \tag{4.34}$$

where

$$\mathbf{x}_{\text{on}}[k] = \begin{bmatrix} x_{\text{on}}^0[k-0] \\ x_{\text{on}}^1[k-0] \\ \vdots \\ x_{\text{on}}^J[k-0] \\ x_{\text{on}}^0[k-1] \\ x_{\text{on}}^1[k-1] \\ \vdots \\ \vdots \\ x_{\text{on}}^J[k-M+1] \end{bmatrix}, \tag{4.35}$$

and the unknown parameter vector is defined as

$$\mathbf{a}_{jm} = \begin{bmatrix} a_{00} & a_{10} & \cdots & a_{(J)0} & a_{01} & a_{11} & \cdots & a_{(J)(M-1)} \end{bmatrix}^T. \tag{4.36}$$

The term $\mathbf{x}_{\text{on}}[k]^T \mathbf{a}_{jm}$ with $\mathbf{x}_{\text{on}}[k] \in \mathbb{R}^{(J+1) \cdot M \times 1}$ and $\mathbf{a}_{jm} \in \mathbb{C}^{(J+1) \cdot M \times 1}$ represents the modeled supply voltage distortion as in (4.26), i.e. $\hat{\alpha}[k] = \frac{\hat{v}_d[k]}{V_{DC}}$.

Putting the samples of $v_{DAC}[k]$ and $x[k]$ together to vectors one can write the output of the RF-DAC in vector-matrix notation

$$\mathbf{v}_{\text{DAC}}[k] = \mathbf{x}[k]\, V_{DC} + \mathbf{D}_x[k] \cdot \mathbf{X}_{\text{on}}[k] \cdot \mathbf{a}_{jm}, \tag{4.37}$$

with

$$\mathbf{v}_{\text{DAC}}[k] = [v_{\text{DAC}}[k]\ v_{\text{DAC}}[k-1]\ \cdots\ v_{\text{DAC}}[k-K+1]]^T, \tag{4.38}$$

and

$$\mathbf{x}[k] = [x[k]\ x[k-1]\ \cdots\ x[k-K+1]]^T. \tag{4.39}$$

Matrices $\mathbf{X}_{\text{on}}[k]$ and $\mathbf{D}_x[k]$ in (4.37) are, respectively, given by

$$\mathbf{X}_{\text{on}}[k] = \begin{bmatrix} \mathbf{x}_{\text{on}}[k]^T \\ \mathbf{x}_{\text{on}}[k-1]^T \\ \vdots \\ \mathbf{x}_{\text{on}}[k-K+1]^T \end{bmatrix}, \tag{4.40}$$

and

$$\mathbf{D}_x[k] = \text{diag}\left(\mathbf{x}[k]\right), \tag{4.41}$$

with $\mathbf{X}_{\text{on}}[k] \in \mathbb{R}^{K \times (J+1) \cdot M}$ and $\mathbf{D}_x[k] \in \mathbb{C}^{K \times K}$. Each row of (4.40) consists of the input samples to the parallel filter structure as in (4.39) for the $[k-i]$-th sample with $i = 0, \ldots, K-1$.

Defining the so-called observation matrix $\mathbf{H}_x[k] = \mathbf{D}_x[k] \cdot \mathbf{X}_{\text{on}}[k]$ finally yields the affine model

$$\mathbf{v}_{\text{DAC}}[k] = \mathbf{x}[k]\, V_{DC} + \mathbf{H}_x[k]\, \mathbf{a}_{jm}. \tag{4.42}$$

Hence, the output of the RF-DAC $\mathbf{v}_{\text{DAC}}[k]$ is linear in the unknown parameter vector $\mathbf{a}_{jm}$ using the model of the supply network distortion as depicted in (4.32). From (4.42), one can thus derive a linear estimator such as the linear (complex-valued) least squares estimator to estimate the unknown coefficient vector [80,83], i.e.

$$\hat{\mathbf{a}}_{jm}[k] = \left[\mathbf{H}_x[k]^H \mathbf{H}_x[k]\right]^{-1} \mathbf{H}_x[k]^H \left(\mathbf{v}_{\text{DAC}}[k] - \mathbf{x}[k]\, V_{DC}\right), \tag{4.43}$$

where $(\cdot)^H$ is the Hermitian transpose, and $\mathbf{v}_{\text{DAC}}[k]$ are the (measured) equivalent baseband data samples of the capacitive RF-DAC's output.

Thus, the proposed SNDPD model in (4.31) with $\alpha[k]$ (4.26) allows to use linear estimation algorithms to determine the parameters a_{jm} from the output of the RF-DAC, similar to the typically used DPD solutions. The SNDPD model is based on the modeling of the effects of a varying supply voltage of the capacitive RF-DAC and therefore does not cover all nonidealities of the RF-DAC. However, estimating parameters a_{jm} by minimizing some cost function of the difference between the output signal and the input signal, as proposed above, inherently considers also some other nonlinearities. As will be shown below, the SNDPD outperforms conventionally used models such as the MP and the GMP, validating the presented supply voltage variations inspired DPD and modeling approach.

4.3.5 Future Development

One further simplification can be utilized if the static nonlinear current mapping, $i_{DD} = g(x_{\mathrm{on}})$, is known a priori. Although this concept was not tested, it looks interesting for future development.

The nonlinear current mapping can be approximated by measuring the average input current $\overline{i_{DD}}$ of the capacitive RF-DAC, as discussed in Section 4.1 and depicted in Figure 4.22. With that, the output based on (4.22) becomes

$$v_{DAC}[k] = x[k] \left(1 + \sum_m h_m \, i_{DD}[k - m] \right), \tag{4.44}$$

which is similar to (4.34) but i_{DD} is known and calculated a priori. Extending this to matrix-vector notation as above yields

$$\mathbf{v}_{\mathrm{DAC}}[k] = \mathbf{H}_{i_{DD}}[k]\,\mathbf{h}[k] + \mathbf{x}[k] \tag{4.45}$$

with

$$\mathbf{h}[k] = [h_0[k]\ h_1[k]\ \cdots\ h_{M-1}[k]]^T \tag{4.46}$$

and the observation matrix

$$\mathbf{H}_{i_{DD}}[k] = \mathrm{diag}\,(\mathbf{x}[k])\ \boldsymbol{\Psi}_{i_{DD}}[k], \tag{4.47}$$

where

$$\boldsymbol{\Psi}_{i_{DD}}[k] = \begin{bmatrix} \mathbf{i}_{DD}[k]^T \\ \mathbf{i}_{DD}[k-1]^T \\ \vdots \\ \mathbf{i}_{DD}[k-K+1]^T \end{bmatrix}. \tag{4.48}$$

with

$$\mathbf{i}_{DD}[k-i] = [i_{DD}[k-i]\ i_{DD}[k-i-1]\ \cdots\ i_{DD}[k-i-K+1]]^T \tag{4.49}$$

Each row of $\boldsymbol{\Psi}_{i_{DD}}[k]$ is composed of the last K average (low-frequency) input current samples at time instance $k - i$, calculated a priori by the static nonlinear function $g(x_{\mathrm{on}})$. The resulting form in (4.45) is equivalent to an affine model.

If the current is known or approximated a priori, the observation matrix $\mathbf{H}_{i_{DD}}[k]$ reduces to a $K \times M$ dimensional matrix instead of a $K \times [(J + 1) \cdot M]$ dimensional matrix as in (4.42) and the unknown parameter vector $\mathbf{h}[k]$ reduces to a $M \times 1$ dimensional vector. Thus, $\mathbf{h}[k]$ represents only the FIR filter taps, modeling the frequency dependent behavior of the supply network.

This significantly reduces the required computational effort for the DPD and the parameter estimation. The model is then equivalent to a (one-dimensional) Hammerstein model with a known static nonlinearity. However, the proposed approach in (4.42) with independent coefficients a_{jm} provides a more general solution to the estimation and predistortion problem.

4.4 Measurement Results of the Supply Network Digital Predistortion

This section discusses the results achieved with the supply network predistortion approach. The figures-of-merit are, as for typical DPD evaluations, the in-band performance in terms of EVM, and the out-of-band performance in terms of ACPR. The proposed approach to suppress the supply network effects is validated with two quadrature capacitive RF-DAC designs: A DPA capacitive RF-DAC [5], and a wideband low-noise quadrature RF-DAC. The DPA connects four capacitive RF-DAC cores to a power combiner to increase the output power up to 25 dBm. Even though the supply network is specifically designed to be very low ohmic, the DPD further reduces the spectral regrowth generated by the nonetheless nonideal supply network. The wideband quadrature capacitive RF-DAC features less output power but provides high linearity and low out-of-band noise emissions for signal bandwidths up to 160 MHz. The design is based on a hybrid quadrature capacitive RF-DAC architecture, similar to [6]. The wideband RF-DAC has a dedicated LDO but the proposed DPD still achieves a significant performance improvement. The EVM could be decreased by almost 6 dB for all applied signal bandwidths and the ACPR is decreased by almost 7 dB in the adjacent channel.

4.4.1 Measurement and Evaluation Setup

The evaluated adjacent channel power is integrated over the same bandwidth as the input signal for the upper and lower adjacent channel, respectively. Thus, for a 20 MHz input signal, the upper out-of-band signal power is integrated over $\Delta f_G + 10\,\text{MHz} \le f \le \Delta f_G + 30\,\text{MHz}$, where Δf_G is a guard band for the respective bandwidth. Reported numbers in the tables below correspond to the lower value of ACPR of either the upper or the lower adjacent channel, respectively.

The measurement setup, similar for both capacitive RF-DACs, is shown in Figure 4.25. The input signal is loaded to an on-chip RAM, which streams the digital code samples to the RF-DAC. A vector signal analyzer (VSA) is connected to the antenna output of the RF-DAC, terminated by a 50 Ω resistor. The VSA also performs the down-conversion from the passband to the equivalent baseband signal, similar to a feedback receiver for on-chip implementations.

The predistortion, and also the estimation of the model coefficients, are performed with MATLAB using the down-converted baseband signal $v_{DAC}[k]$ from the VSA. The down-converted output signal is normalized by the expected linear RMS gain of the RF-DAC g_{rms} and further time (Δt) and phase ($\Delta\varphi$) synchronized to the input data as indicated in Figure 4.25. The direct and the indirect learning methods have been applied [10], using the complex-valued least-squares estimator (4.43) as estimation algorithm. Coefficient estimation and predistortion of the input signal are both combined in the DPD block in Figure 4.25.

The performance of the SNDPD is compared to the memory polynomial [24] and the generalized memory polynomial [21]. In contrast to the MP and the GMP the

SNDPD explicitly uses the equivalent number of active switching cells $x_{\text{on}}[k]$ as input to the predistorter, corresponding to the dependency of the supply voltage distortion on the number of active switching cells as discussed in Section 4.1.2. Both measured RF-DACs are based on a quadrature architecture and hence the input to the SNDPD is $x_{\text{on}}[k] = |x_I[k]| + |x_Q[k]|$, whereas MP and GMP use the magnitude $|x[k]|$.
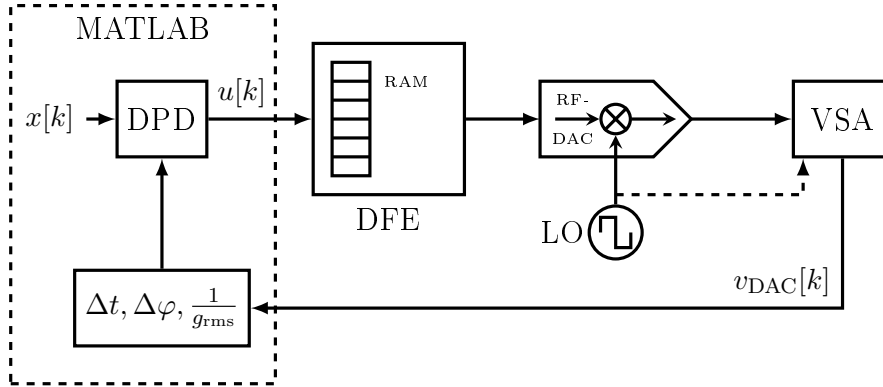
Figure 4.25: Measurement setup for DPD evaluation.

Figure 4.26 shows the difference between input signal and down-converted output signal of the VSA of the wideband capacitive RF-DAC without DPD. The achievable noise floor of all measurements is limited to approximately $-135\,\text{dBm/Hz}$ due to accuracy of the measurement equipment, i. e. phase-noise of the LO (clock) generator.
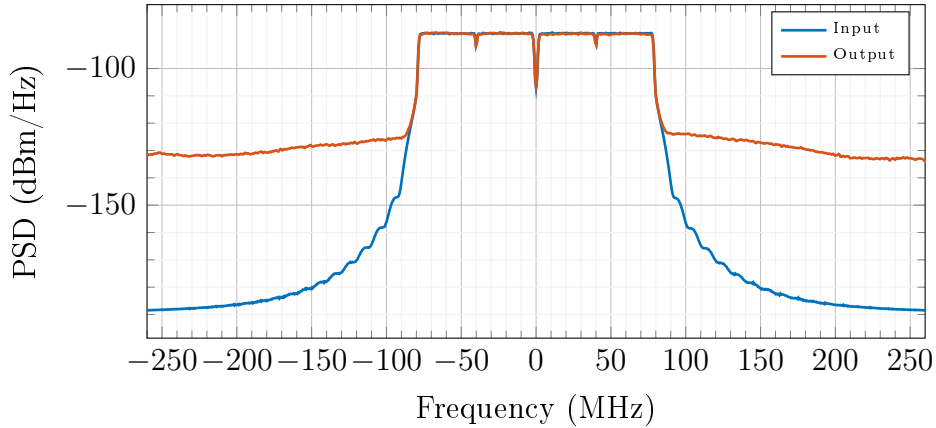
Figure 4.26: PSDs of the input signal and the output signal of the capacitive RF-DAC. The achievable minimum noise floor is limited by the phase-noise of the used LO (clock) generator.

4.4.2 DPA Measurement Results

The bandwidth of the used VSA's internal down-conversion filter was limited to 40 MHz, thus limiting the available bandwidth for predistortion. Nevertheless, measurements with signal bandwidths up to 15 MHz are still feasible. The parameters of the DPD are estimated by using the indirect learning approach as given in (2.84). Only one iteration is performed. The DPA is supplied by an ideal (non-switching) voltage source.

Here, the SNDPD (4.32) is compared to the memory polynomial (2.66b). Both models are given here again:

$$u_{\text{SNDPD}}[k] = x[k] \left(1 - \sum_{m=0}^{M-1} \sum_{j=1-L}^{J-1} a_{jm}\, x_{\text{on}}^{j}[k-m] \right), \tag{4.50}$$

$$u_{\text{MP}}[k] = \sum_{j=1-L}^{J-1} \sum_{m=0}^{M-1} a_{jm}\, x[k-m]\, |x[k-m]|^{j} \tag{4.51}$$

where J defines the order of the polynomial and M is the filter length. The parameter L defines if the models include the linear terms. For $L = 0$ the memory polynomial includes so-called linear memory terms, i.e. $\sum_m a_{0m}\, x[k]$. In contrast, the SNDPD model becomes $x[k]\,(1 - \sum_m a_{0m})$, which simply adds a constant term to $u[k]$. Therefore the MP has more degrees of freedom if $L = 0$.

Figure 4.27 shows the output spectrum of the DPA with and without the proposed supply network predistortion, using a polynomial of order $J = 3$ and $M = 4$ memory taps. The in-band signal power is approximately 7.5 dBm. With the supply network DPD approach, the power in the adjacent channel is reduced by almost 5 dB as listed in Table 4.27b. The supply network of the DPA is designed to be very low ohmic, being even competitive to a high-performance LDO. Nevertheless, the proposed supply network DPD significantly reduces out-of-band emissions.

Figure 4.28 shows the comparison of the predistortion performance with and without memory taps in the FIR filter, i.e. comparing a memory-based DPD to a pure instantaneous (static) DPD approach. Both cases use a third-order polynomial. The results show that already for a 15 MHz input signal, a memory-based DPD is superior to a pure instantaneous model. Henceforth, using memory in the applied DPD is crucial for signals with higher bandwidth. Nevertheless, too many filter taps can have a negative effect as estimation errors due to the overdetermined model are introduced. This results in an increased noise floor in the far-out-of band regions as depicted in Figure 4.29 for a 5 MHz LTE signal. Using eight memory taps shows almost no performance increase in the close out-of-band region, but causes higher spectral regrowth in the far out-of-band region. Thus, for signals with small bandwidth, reducing memory taps achieves a more robust performance.

Figure 4.30 shows the comparison of the SNDPD and the memory polynomial approach. It can be seen that the SNDPD achieves similar performance compared to the memory polynomial, although complexity is lower. It will be shown in

(a)
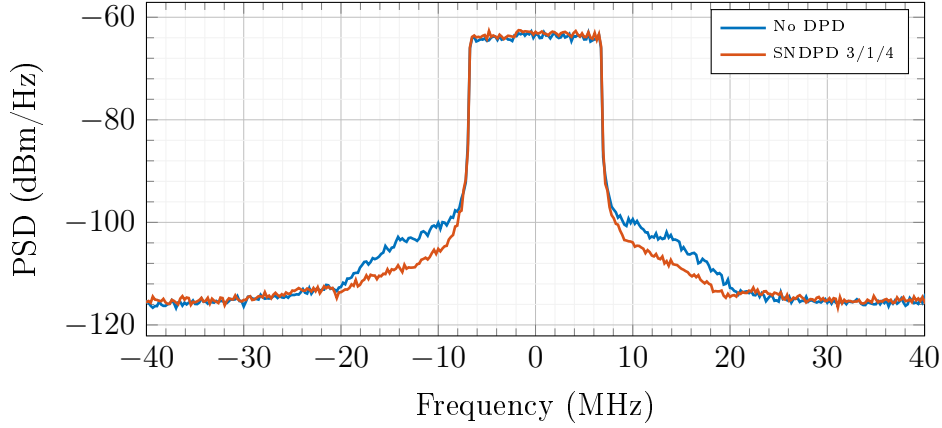
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	7.48	-40.81
SNDPD	3/1/4	7.94	-45.13

(b)

Figure 4.27: Capacitive RF-DAC output spectrum for a 15 MHz LTE signal with and without SNDPD.

(a)
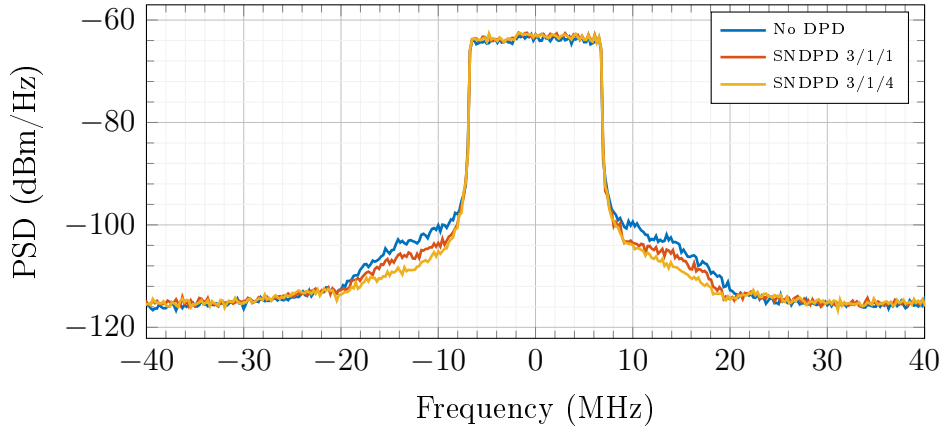
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	7.48	-40.81
SNDPD	3/1/1	7.97	-43.77
SNDPD	3/1/4	7.94	-45.13

(b)

Figure 4.28: PSD and key parameters of 15 MHz LTE signals without DPD and with DPD using $M = 1$ and $M = 4$ FIR filter taps.

Section 4.4.3 that for high bandwidth signals, i.e. 80 MHz and beyond, the supply network DPD approach even outperforms the state-of-the-art used memory-based DPD approaches.

(a)
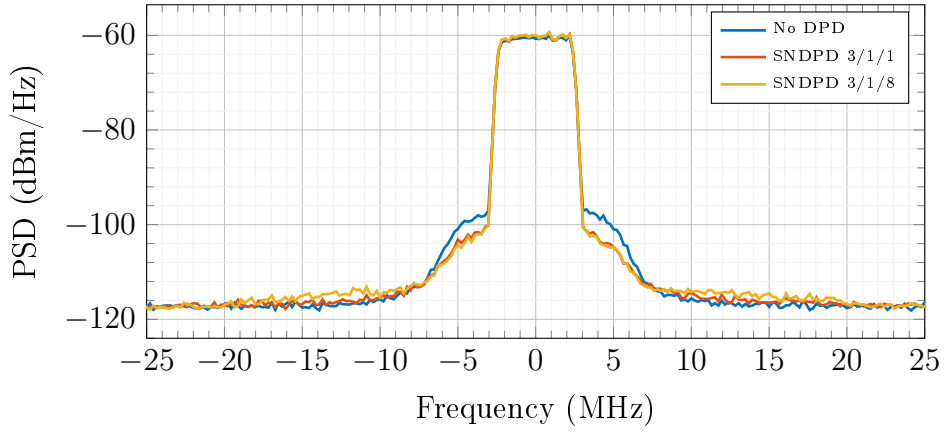
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	6.10	-41.88
SNDPD	3/1/1	6.48	-45.56
SNDPD	3/1/8	6.52	-46.14

(b)

Figure 4.29: PSDs and key parameters of 5 MHz LTE signals without DPD and with DPD using $M = 1$ and $M = 8$ FIR filter taps.

(a)
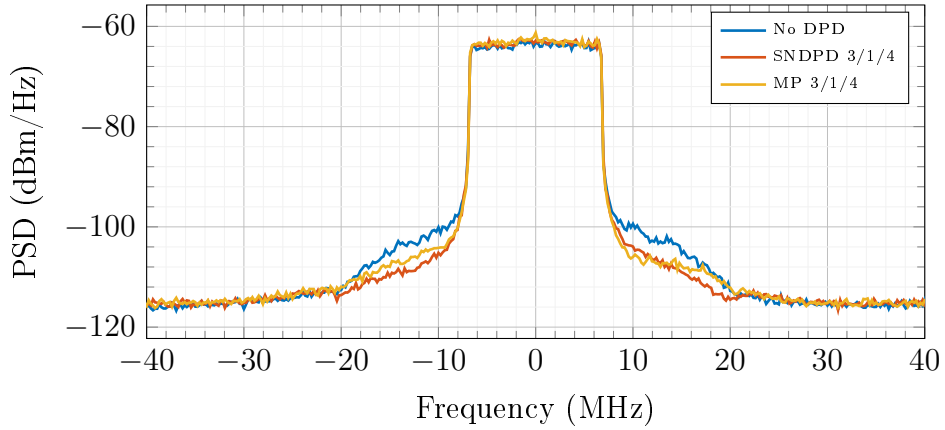
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	7.48	-40.81
MP	3/1/4	8.21	-44.52
SNDPD	3/1/4	7.94	-45.13

(b)

Figure 4.30: PSD and key parameters of 15 MHz LTE signals without DPD, with supply network DPD, and with memory polynomial DPD.

Typical used predistortion approaches often neglect the second-order term, based on the derivation of the equivalent baseband model of the Volterra series [7]. How-

ever, supply network distortions show a second-order nonlinear behavior due to the static nonlinear relation of the code-to-current mapping, as discussed in Section 4.1 and sketched in Figure 4.22. The second-order distortion is the main contributor to the spectral regrowth and can be utilized in the SNDPD approach. Figure 4.31 shows the PSD of the capacitive RF-DAC output for different polynomial orders. As expected, a predistortion with only a purely linear function, i. e. $J = 1, L = 1$, does not affect the spectral regrowth. However, by just using the second-order non-linearities, i.e. $J = 2$, the achieved suppression of the adjacent channel power by the SNDPD is almost equivalent as when using third-order, $J = 3$, nonlinearities. Hence, the complexity can be further reduced to a second-order implementation, fortifying that a predistortion model considering the main contributors of a known circuit design can achieve similar or better results to state-of-the-art black-box models.

(a)
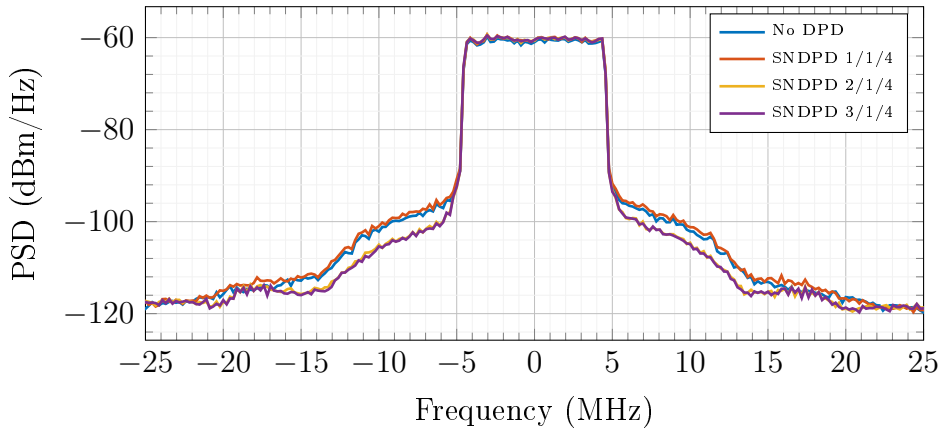
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	8.76	-40.57
SNDPD	1/1/4	9.20	-40.21
SNDPD	2/1/4	9.20	-43.99
SNDPD	3/1/4	9.21	-44.07

(b)

Figure 4.31: PSDs and key parameters of 10 MHz LTE signals with and without DPD for different polynomial orders $J = \{1, 2, 3\}$.

Besides the ACPR, also the in-band performance is affected by the nonlinearities. For multi-carrier modulations such as OFDM, second-order and third-order distortions of the lower frequency tones cause distortions in the in-band signal region, degrading the EVM. Figure 4.32 depicts the estimated EVM over the output signal power without predistortion, with memory polynomial, and with supply network DPD, respectively. Both DPD approaches use a polynomial order of $J = 3$ and $M = 4$ memory taps. The input signal is a 20 MHz, 64-QAM modulated OFDM signal. The coefficients are estimated once at 14 dBm output power and then used over the whole input signal power range. The SNDPD again outperforms the

memory polynomial by approximately 1 dB over the whole output range. At the trained output power, the SNDPD decreases the EVM by almost 4 dB. In typical system integrations, a set of different DPD coefficients would be used dependent on the output signal power. The respective output and input signal spectrum for 6 dBm (in-band signal power) is shown in Figure 4.32b.
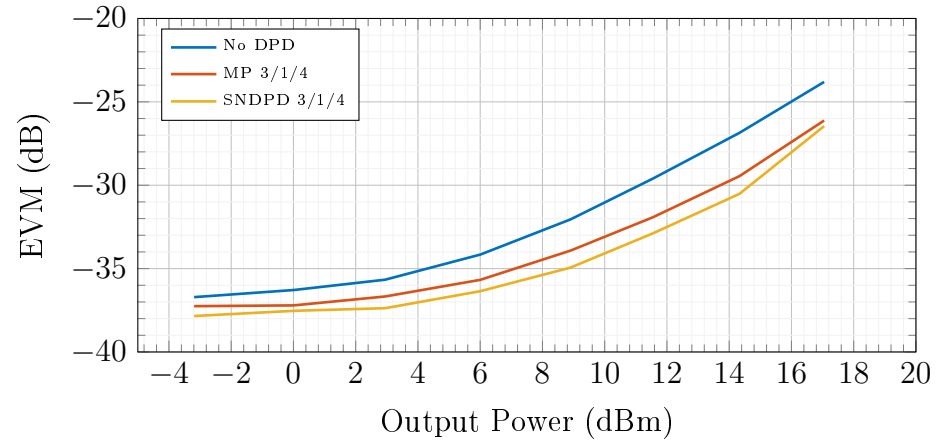
(a)
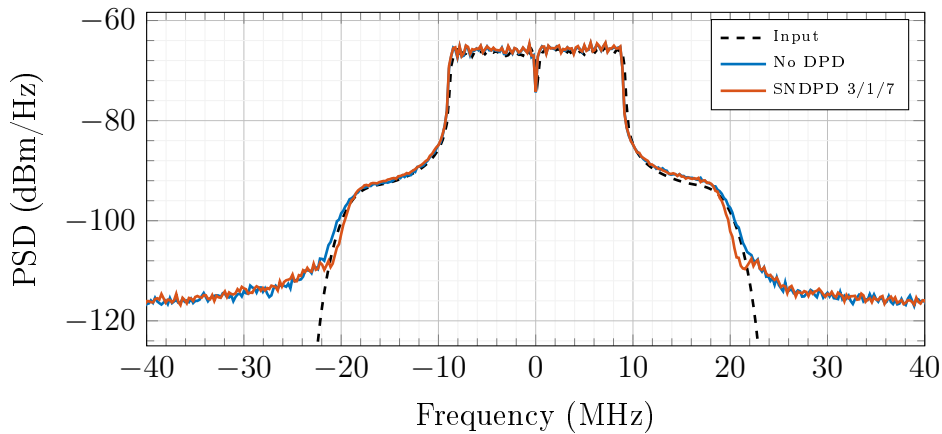
(b)

Figure 4.32: Comparison of SNDPD and MP for a 20 MHz input signal. (a) EVM, (b) PSD of capacitive RF-DAC output.

4.4.3 Wideband Capacitive RF-DAC Measurement Results

Compared to the DPA, the wideband quadrature capacitive RF-DAC is designed for less output power. However, high linearity and minimized out-of-band noise floor is achieved even without DPD, reducing the spectral regrowth compared to the DPA. Furthermore, due to increasing EVM requirements for the latest communication standards such as 5G and Wi-Fi 6, also the in-band performance

is improved. However, predistortion still improves the performance of the RF-DAC.

Another distinction to the DPA is the supply network. An internal LDO regulator is used to compensate for DC-DC voltage ripple and the signal dependent current feedback. However, the LDO is not designed to track the applied high bandwidth signals and thus the supply network effects degrade the ACPR.

The bandwidth of the used VSA for these measurements is 600 MHz, which allows to validate the DPD for signal bandwidths up to 160 MHz.

Contrary to the DPA measurements, the direct and the indirect learning methods are applied, using indirect learning for the initial calibration, followed by three iterations of using direct learning to update the coefficients [115].

Here, the performance of the SNDPD is compared to the MP and the GMP. The implemented realizations are given by

$$
u_{\mathrm{SNDPD}}[k] = \sum_{m=0}^{M_{\mathrm{lin}}-1} a_{0m}\, x[k-m]
$$
$$
- \left(x[k] \cdot \sum_{m=0}^{M-1}\sum_{j=1}^{J-1} a_{jm}\, x_{\mathrm{on}}^{j}[k-m] \right), \tag{4.52}
$$

$$
u_{\mathrm{MP}}[k] = \sum_{m=0}^{M_{\mathrm{lin}}-1} a_{0m}\, x[k-m]
$$
$$
+ \sum_{j=1}^{J-1}\sum_{m=0}^{M-1} a_{jm}\, x[k-m]\,|x[k-m]|^{j}, \tag{4.53}
$$

$$
u_{\mathrm{GMP}}[k] = \sum_{m=0}^{M_{\mathrm{lin}}-1} a_{0m}\, x[k-m]
$$
$$
+ \sum_{j=1}^{J-1}\sum_{m=0}^{M-1} a_{jm}\, x[k-m]\,|x[k-m]|^{j}
$$
$$
+ \sum_{j=1}^{J-1}\sum_{m=0}^{M-1}\sum_{n=1}^{N_{\mathrm{lag}}} b_{jmn}\, x[k-m]\,|x[k-m-n]|^{j}
$$
$$
+ \sum_{j=1}^{J-1}\sum_{m=0}^{M-1}\sum_{n=1}^{N_{\mathrm{lead}}} d_{jmn}\, x[k-m]\,|x[k-m+n].|^{j}. \tag{4.54}
$$

The parameters are summarized as follows:

- J defines the highest order of the nonlinearity.

- M defines the number of used memory taps for the nonlinear terms.

- M_{lin} defines the number of memory taps for the linear term represented by the first row of each DPD model above.

- N_{lag} and N_{lead} define the number of off-diagonal elements of the GMP.

In the results shown below, the parameter L defines if the linear memory terms are included in the DPD, i.e.

$$L = \begin{cases} 0 & \dots M_{\text{lin}} = 1 \\ 1 & \dots M_{\text{lin}} = M \end{cases} \tag{4.55}$$

Thus, if $L = 1$, the linear memory is included. Depending on the individual definitions in the literature the MP and the GMP can inherently include linear memory terms. However, the SNDPD model as defined in (4.32) does not account for these terms. To provide a better comparison these linear terms are additionally included in the SNDPD. For $L = 0$, i.e. $M_{\text{lin}} = 1$, the SNDPD in (4.52) becomes again the proposed approach as in (4.32). However, as is shown below, including the linear memory terms improves the performance of the SNDPD for the measured RF-DAC.

Figure 4.33 shows the PSD of the capacitive RF-DAC's output for 802.11ac Wi-Fi signals with 20 MHz, 80 MHz, and 160 MHz bandwidth without any predistortion, respectively. It can be seen, that for a 20 MHz signal, the out-of-band emissions are very low, resulting from the linear design of the RF-DAC. Furthermore, the LDO supports still enough gain for the 20 MHz input signals, suppressing the effects of the supply current variations. However, for signals with higher bandwidth, i.e. 80 MHz and 160 MHz, the spectral regrowth increases significantly. The key parameters are summarized in Table 4.33b. Although spectral regrowth is low for 20 MHz, the EVM is similar to the high bandwidth signals.

Figure 4.34 shows the PSD and the respective key parameters for a 20 MHz Wi-Fi 802.11ac modulated signal with and without predistortion. The SNDPD is compared to the generalized memory polynomial. Visually, there is only a marginal benefit of the DPD in terms of suppressing the spectral regrowth for a 20 MHz signal. However, the integrated out-of-band power shows that the ACPR can still be improved by almost 2 dB. Nevertheless, a significant performance boost of almost 6 dB in the EVM can be achieved by using predistortion. The SNDPD approach is even outperforming the GMP, although its complexity is only a fraction compared to the GMP. Furthermore, by just using a second-order polynomial for the SNDPD, the EVM can be significantly improved and almost achieves the performance compared to higher order nonlinear models.

Figure 4.35 depicts the comparison of the different predistortion approaches for an 80 MHz 802.11ac Wi-Fi signal. The SNDPD approach clearly outperforms the MP and the GMP with $N_{\text{lead}} = N_{\text{lag}} = 1$. GMP and MP show a higher noise floor as shown in Figure 4.35a. The increased noise floor of the GMP and MP is caused by estimation errors for the higher number of used basis functions. For the GMP this causes small humps as can be seen in the spectrum at ± 100 MHz. However, the ACPR can still be improved by almost 5 dB. In contrast, the SNDPD is robust for the same polynomial and memory order as the MP and GMP. Moreover, the
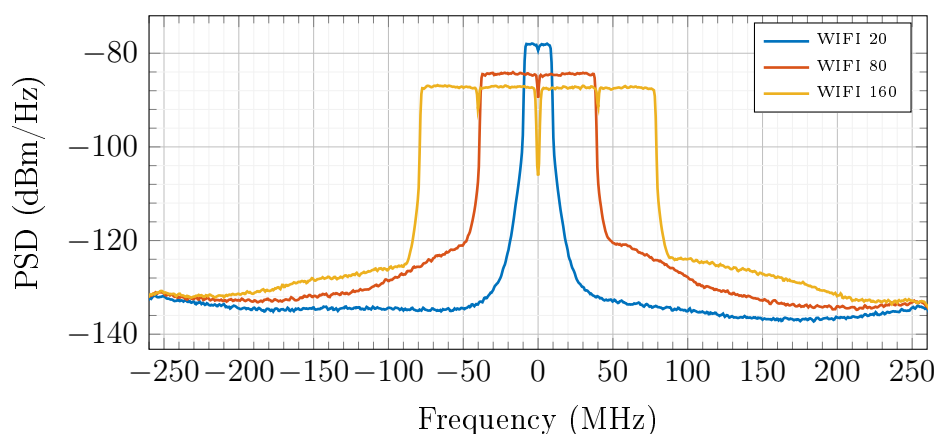
(a)

Bandwidth (MHz)	Output Power (dBm)	EVM (dB)	ACPR (dB)
20	-5.68	-34.50	-43.72
80	-5.68	-33.83	-39.94
160	-5.49	-34.82	-39.78

(b)

Figure 4.33: PSD of the capacitive RF-DAC's output for 802.11ac Wi-Fi signals with 20 MHz, 80 MHz, and 160 MHz bandwidth without predistortion.

(a)
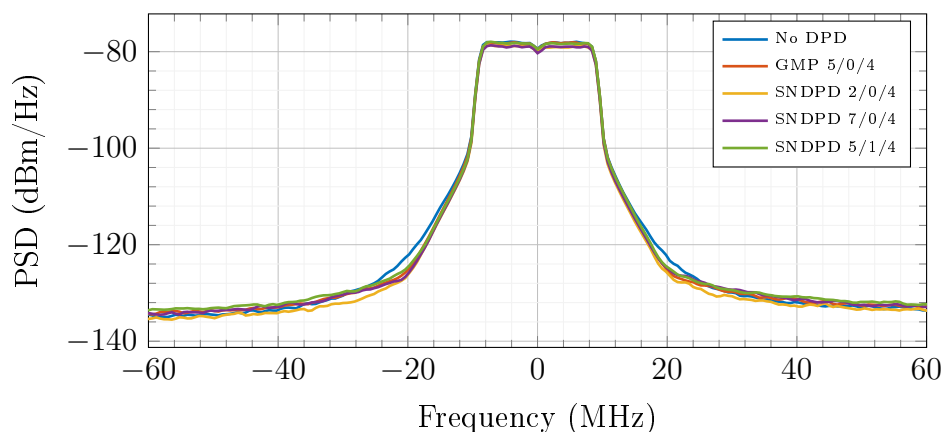
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.68	-34.50	-43.72
GMP	5/0/4	-5.81	-39.68	-45.41
SNDPD	2/0/4	-6.44	-38.94	-45.64
SNDPD	7/0/4	-6.51	-39.32	-44.73
SNDPD	5/1/4	-5.81	-40.29	-45.07

(b)

Figure 4.34: PSDs and key parameters of 20 MHz OFMD modulated signals with and without DPD.

SNDPD even achieves comparable performance with only a second-order nonlinearity used in the DPD model. This indicates the relation of the SNDPD model to the actual behavior of the supply network, which shows a quadratic-like behavior, as shown in Figure 4.22. In contrast to the MP and GMP, which use the magnitude $|x[k]|$, the SNDPD uses the sum of magnitudes, i.e. $x_{on} = |x_I[k]| + |x_Q[k]|$, as input to the predistorter. As will be shown below, also the MP performance can be increased by using x_{on}. The EVM can be improved by more than 5 dB and the ACPR by almost 7 dB as shown in Table 4.35b.

(a)
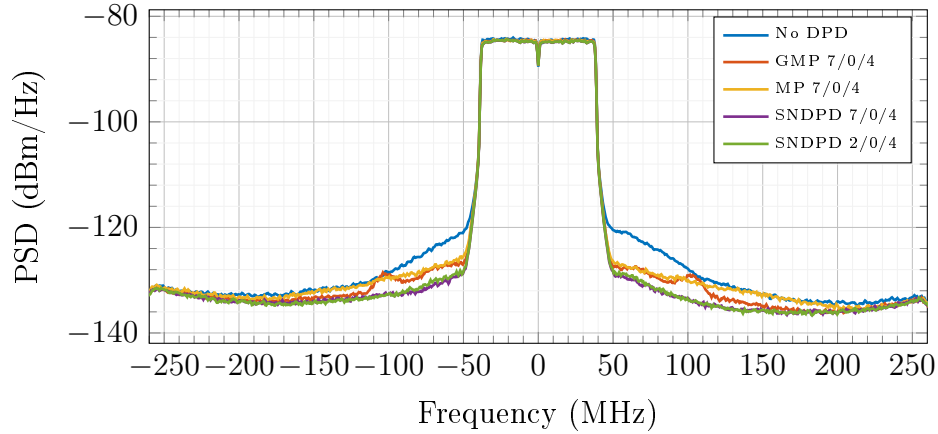
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.68	-33.83	-39.94
GMP	7/0/4	-5.83	-38.26	-44.33
MP	7/0/4	-5.86	-39.02	-43.74
SNDPD	7/0/4	-6.01	-39.03	-46.73
SNDPD	2/0/4	-5.99	-39.02	-46.40

(b)

Figure 4.35: PSDs and key parameters of 80 MHz OFMD modulated signals. Comparison between generalized memory polynomial, memory polynomial, and supply network DPD.

Figure 4.36 shows the performance of the SNDPD approach for different coefficient sets for a 160 MHz input signal. Adding the linear terms in the DPD, i.e. $L = 1$, improves the ACPR by additional 2 dB. Additionally, also the number of filter taps is increased to 14. However, this only shows a minor impact on the DPD performance. Empirical investigations showed that the best performance can be achieved with $J = 5, L = 1$, and $M = 4$, improving the EVM and ACPR by around 5 dB, while still keeping the complexity low. At distinct frequency bins the spectral leakage could be decreased by almost 12 dB.

Another interesting comparison is shown in Figure 4.37. The SNDPD approach is compared to the memory polynomial for a 160 MHz 802.11ac Wi-Fi signal. Here, the linear term is now also used in the MP. Furthermore, the I/Q case uses the sum of magnitudes, i.e. $x_{on}[k]$, as input to the nonlinear terms of the MP, equivalent

(a)

DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.49	-34.82	-39.78
SNDPD	5/0/4	-5.61	-39.17	-42.72
SNDPD	5/1/4	-5.70	-39.77	-44.81
SNDPD	5/1/14	-5.64	-39.89	-44.43

(b)

Figure 4.36: PSDs (a) and key parameters (b) of 160 MHz OFMD modulated signals. Comparison between different coefficient sets of the supply network DPD approach.

to the SNDPD. Including the linear terms and using the sum of magnitudes for the MP results in almost the same improvement of the EVM and the ACPR as compared to the SNDPD, as shown in Table 4.37b. This indicates that the nonlinear characteristic of the quadrature capacitive RF-DAC is dominated by sum of magnitudes $|x_I[k]| + |x_Q[k]|$ rather than by the magnitude $|x[k]|$, corresponding to the derived dependency of the supply network variations on the number of active switching cells $x_{\mathrm{on}}[k]$, as discussed in Section 4.1.

Figures 4.38 and 4.39 present the SNDPD results for 80 MHz and 160 MHz signals, respectively. The signals are composed of four/eight parallel 20 MHz LTE signals in the frequency domain. The results in Table 4.38b show that the ACPR can be significantly improved by almost 8 dB. Figure 4.38 again shows that the SNDPD with only a second-order polynomial almost achieves the same results as with a seventh-order polynomial. The ACPR differs only by approximately 0.3 dB. Figure 4.39 depicts the results achieved by different coefficient sets when using the SNDPD approach. Similar to the Wi-Fi signals, the linear part in the DPD algorithm, i.e. $L = 1$, improves the performance by almost 2 dB.

Figure 4.40 shows three iteration steps of the coefficient estimation for the SNDPD with $J = 5, L = 1, M = 4$ using a 160 MHz 802.11ac Wi-Fi signal. The DPD already achieves a significant improvement after the first iteration, using indirect learning. Additional iterations only have a minor impact on the ACPR and the EVM, which most probably result from the limited accuracy of the measurement setup.

(a)

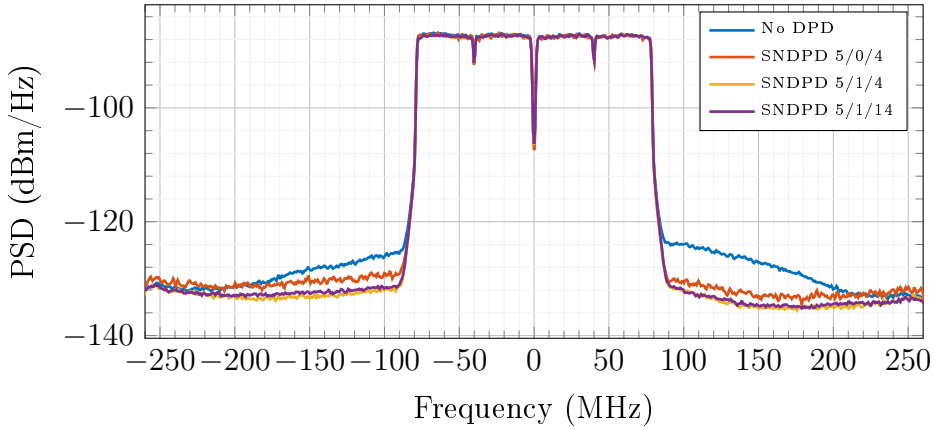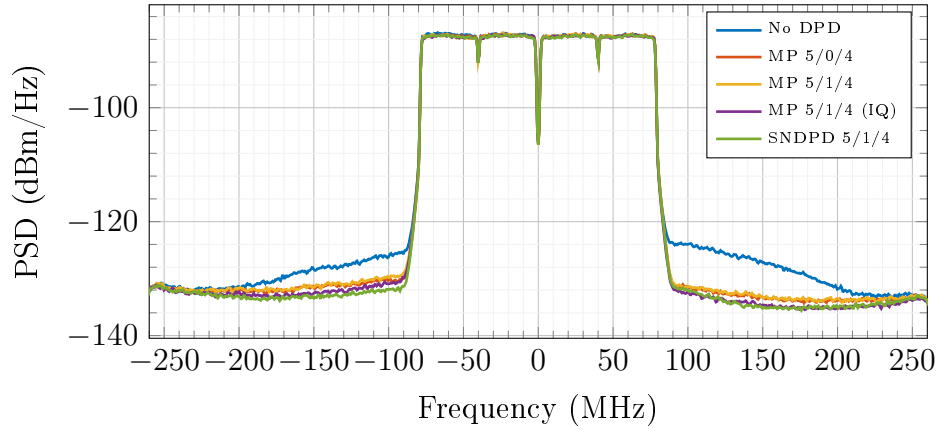| DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	0/0/0	-5.49	-34.82	-39.78
MP	5/0/4	-5.57	-39.32	-43.68
MP	5/1/4	-5.59	-39.37	-43.35
MP	5/1/4 (I/Q)	-5.69	-39.68	-44.20
SNDPD	5/1/4	-5.70	-39.77	-44.81

(b)

Figure 4.37: PSDs and key parameters of 160 MHz OFMD modulated signals. Comparison between memory polynomial and supply network DPD.

(a)
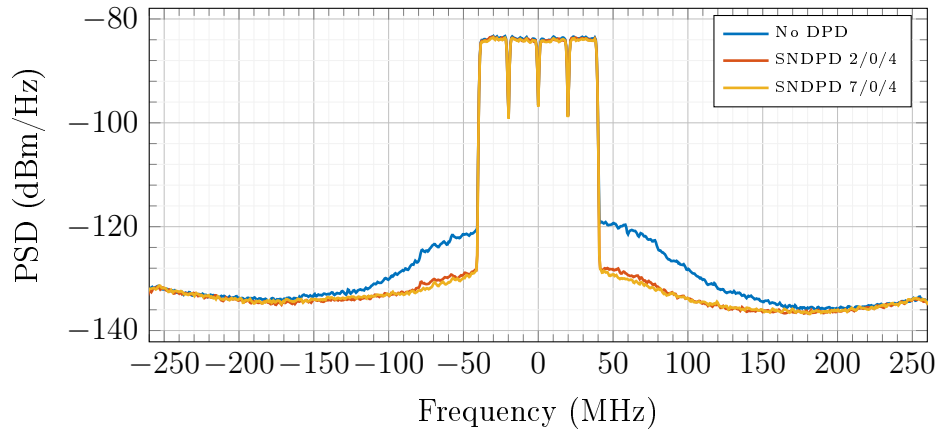
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	-5.18	-39.94
SNDPD	2/0/4	-5.35	-47.40
SNDPD	7/0/4	-5.48	-47.71

(b)

Figure 4.38: PSDs and key parameters of a 4×20 MHz LTE signal. Comparison between different coefficient sets of the supply network DPD.

(a)
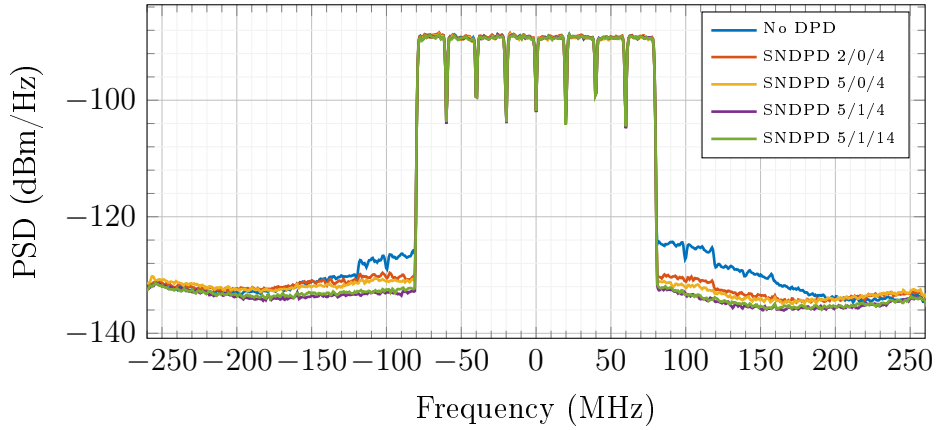
DPD type	Coefficient Set ($J/L/M$)	Power (dBm)	ACPR (dB)
No DPD	0/0/0	-7.56	-39.66
SNDPD	2/0/4	-7.48	-41.91
SNDPD	5/0/4	-7.68	-42.04
SNDPD	5/1/4	-7.67	-43.64
SNDPD	5/1/14	-7.67	-43.35

(b)

Figure 4.39: PSDs and key parameters of a 8×20 MHz LTE signal. Comparison between different coefficient sets of the supply network DPD.
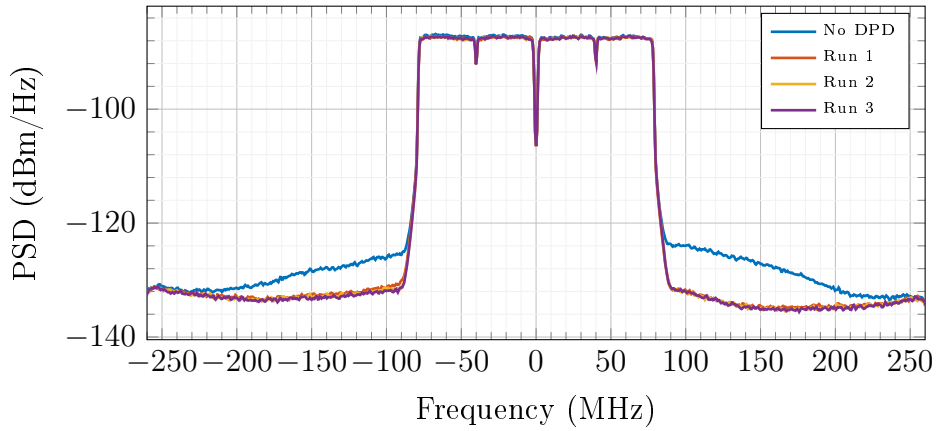
(a)

Run	Learning	Power (dBm)	EVM (dB)	ACPR (dB)
No DPD	none	-5.49	-34.82	-39.78
Run 1	indirect	-5.70	-39.86	-44.39
Run 2	direct	-5.72	-39.81	-44.65
Run 3	direct	-5.70	-39.77	-44.81

(b)

Figure 4.40: PSDs and key parameters of a 160,MHz Wi-Fi signal for three coefficient learning iterations, using the supply network DPD approach with $J = 5, L = 1, M = 4$.

Figure 4.41 additionally depicts the respective AM-AM and AM-PM plots without DPD and with SNDPD. The performance, especially for the AM-PM, indicates the limits of the phase noise of the external LO generator.

Figure 4.41: AM-AM and AM-PM of measured wideband RF-DAC without DPD and with SNDPD with $J = 5, L = 1, M = 4$. The performance was limited by the measurement setup, i.e. the phase-noise of the LO (clock) generator.

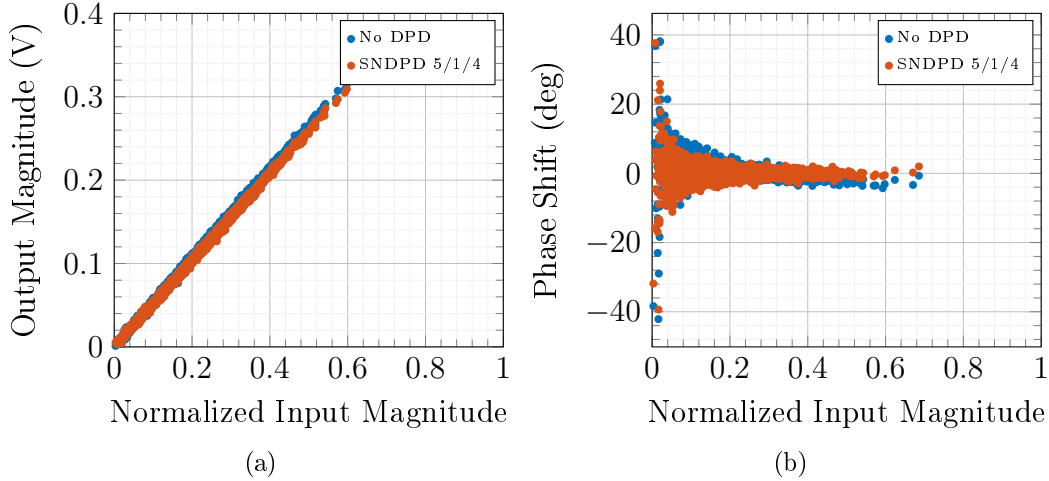The presented measurement results validate that the SNDPD is an effective method to significantly improve the ACPR and the EVM of capacitive RF-DACs. Due to the physical inspired modeling approach of the RC-DAC's non-idealities, the proposed SNDPD allows for a feasible implementation on an integrated circuit while even outperforming conventional DPD models such as the (generalized) memory polynomial.

4.5 Discussion

This chapter discussed the effect and the means to compensate the effects of an imperfect supply network for capacitive RF-DACs using digital predistortion.

A nonideal supply voltage, distorted either by deterministic effects such as DC-DC converter voltage ripples or by random fluctuations caused by code dependent voltage drop over an imperfect supply network, severely decrease the linearity of the capacitive RF-DAC. This causes the in-band performance, i.e. the EVM, and the out-of-band performance in terms of spectral regrowth to degrade.

The proposed supply network DPD is based on the physical behavior of the circuit's internals and outperforms typically used black-box approaches such as the (generalized) memory polynomial. The input of the SNDPD depends on the normalized number of active switching cells $x_{\text{on}}[k] = O_n(x[k])$, changing with the used RF-DAC architecture. This approach differs compared to the typically used DPD models such as the MP, the GMP, and the EMP which always use the magnitude of the baseband input signal $|x[k]|$. In general, the SNDPD can be seen

as a special case of the GMP (similar to the EMP) which only uses the relevant basis functions corresponding to nonlinear effects caused by the nonideal supply network. This also yields a more robust behavior of the SNDPD model compared to the GMP even when using higher polynomial orders and a larger set of memory taps.

Measurement results proofed the concept and its performance. Two capacitive RF-DAC implementations were used for validation, where for both systems the SNDPD significantly decreases the EVM and the spectral regrowth. The EVM could be decreased by almost 6 dB for all signal bandwidths. The ACPR is also decreased by up to 7 dB. For dedicated frequency bins the spectral emission is even reduced by up to 12 dB.

The DPD approach for cancellation of the DC-DC voltage ripples was presented to the circuits and systems community [108]. The supply network predistortion approach for capacitive RF-DACs was filed with the US patent office and granted in 2018 [113]. Additionally, a journal paper of the SNDPD approach has been submitted to the IEEE Transactions on Microwave Theory and Techniques and is currently under review.

5 Conclusion

This thesis addressed the modeling and digital predistortion for capacitive RF-DACs. The introduced modeling approach using switched state-space models is an efficient method to simulate internal as well as external non-idealities of the capacitive RF-DAC architecture. The digital predistortion cancels the effects of a varying supply voltage on the RF-DAC's output by using a modified parallel Hammerstein model approach, enabling to reduce the stringent requirements of the supply network or improve the linearity of the RF-DAC.

The presented simulation model utilizes a close-to-circuit relation, allowing to simulate and analyze individual, undesired contributors to the nonlinear behavior of the RF-DAC. First approaches using switched linear state-space models provide a fast way of simulating the RF-DAC by using the desired component values of the design. However, internal non-idealities such as the AM-PM distortion cannot fully be covered. Thus, the switched linear state-space model was extended to the switched nonlinear state-space model, covering the AM-PM distortion introduced by voltage-dependent on-resistances of NMOS/PMOS transistors in the driving inverters of the capacitive RF-DAC cells. Furthermore, extensions to the switched state-space approach for capacitive RF-DAC modeling, covering crucial non-idealities such as capacitor mismatch, supply voltage variations, and LO phase noise were discussed. The model achieves a good match compared to SpectreRF® simulations and measurements while reducing the simulation run-time by a factor of more than 100.

The proposed supply network digital predistortion approach employs the knowledge of the physical behavior of the RF-DAC's behavior and its supply network. The DPD concept recreates the voltage distortions on the capacitive RF-DAC supply and utilizes this information to modulate the input code to compensate the distortions on the output signal of the capacitive RF-DAC. Computational complexity is brought down to a feasible level, enabling an efficient implementation. The concept was validated by measures taken on two capacitive RF-DAC architectures. Furthermore, the SNDPD measurements were compared to state-of-the-art DPD approaches such as the generalized memory polynomial and achieves better performance with even a reduced number of coefficients. By applying the SNDPD the adjacent channel leakage ratio over the same bandwidth as the transmitted signal is improved by up to 7 dB for signals up to 160 MHz. For close out-of-band frequencies the spectral regrowth is reduced by up to 12 dB. Moreover, also the in-band linearity, i.e. the EVM, could be improved by almost 6 dB.

A Derivations of Nonlinear Models and DPD

A.1 Example to define Volterra Kernel

This section gives an example of how Volterra kernels can be related to a nonlinear system. The system is assumed to be composed of a LTI system, followed by a memoryless nonlinear system, i. e. a Wiener model. The LTI system is defined by its impulse response $h(t)$ and the memoryless nonlinearity by a 2-nd order polynomial. The output of the LTI system is thus given by

$$y(t) = \int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau. \tag{A.1}$$

The output of the polynomial is defined as

$$z(t) = a_0 + a_1\, y(t) + a_2\, y^2(t). \tag{A.2}$$

Hence the total system can be described by

$$
\begin{aligned}
z(t) &= a_0 + a_1 \int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau + a_2 \left[\int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau \right]^2 \\
&= a_0 + a_1 \int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau \\
&\quad + a_2 \left[\int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau \right] \left[\int_{-\infty}^{\infty} h(\tau)\, x\,(t - \tau)\ d\tau \right] \\
&= a_0 + \int_{-\infty}^{\infty} a_1 h(\tau_1)\, x\,(t - \tau_1)\ d\tau_1 \\
&\quad + \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} a_2\, h\,(\tau_1)\, h\,(\tau_2)\, x\,(t - \tau_1)\, x\,(t - \tau_2)\ d\tau_1\, d\tau_2 \tag{A.3}
\end{aligned}
$$

where the kernels of the Volterra series can be defined as

$$h_0 = a_0, \tag{A.4a}$$

$$h_1(\tau_1) = a_1 \, h(\tau_1), \tag{A.4b}$$

$$h_2(\tau_1, \tau_2) = a_2 \, h(\tau_1) \, h(\tau_2). \tag{A.4c}$$

The system is thus fully described by the Volterra kernels.

A.2 Convergence of Volterra Series

Similar to A.1 above, assume a system composed of an LTI system, followed by a memoryless nonlinearity [26]. The output of the LTI system is given by

$$y(t) = \int\limits_{-\infty}^{\infty} h(\tau) \, x\,(t - \tau) \; d\tau. \tag{A.5}$$

The output of the memoryless nonlinearity is

$$z(t) = \frac{y(t)}{1 + y^2(t)}, \tag{A.6}$$

which can be expanded into a Taylor series of the form

$$z(t) = \sum_{n=0}^{\infty} (-1)^n \, [y(t)]^{2n+1} \,. \tag{A.7}$$

The Volterra operator is then defined by

$$z(t) = \sum_{n=0}^{\infty} (-1)^n \left[\int\limits_{-\infty}^{\infty} h(\tau) \, x\,(t - \tau) \; d\tau \right]^{2n+1} \tag{A.8a}$$

$$= \sum_{n=0}^{\infty} H_{2n+1} \, [x(t)] \,, \tag{A.8b}$$

where the dedicated Volterra kernel is given by

$$h_{2n+1}\,(\tau_1, \tau_2, \ldots, \tau_{2n+1}) = (-1)^n \, h\,(\tau_1) \cdots h\,(\tau_{2n+1}) \tag{A.9}$$

The Taylor series expansion in (A.7) only converges if $|y(t)| < 1$. Henceforth the Volterra series diverges for $|y(t)| > 1$ and is thus only valid for input signals $x(t)$ which guarantee the output of the LTI system to be $|y(t)| < 1$.

A.3 Comparison of SNDPD and EMP

This section shows that the SNDPD for the polar case is equivalent to the EMP. Here, only the equivalent baseband signals are considered, thus omitting the tilde symbol.

The SNDPD using the parallel filter approach is defined as

$$u[k] = x[k] \left(1 - \sum_{m=0}^{M-1} \sum_{j=0}^{J} a_{jm} \, x_{\text{on}}^{j}[k - m] \right). \tag{A.10}$$

For the polar architecture, the input to the parallel filter structure is equal to the magnitude of the baseband signal, i.e. $x_{\text{on}}[k] = |x[k]|$. Thus the predistorter is given by

$$u[k] = x[k] \left(1 - \sum_{m=0}^{M-1} \sum_{j=0}^{J} a_{jm} \, |x[k - m]|^{j} \right). \tag{A.11}$$

Separating now the case for $j = 0$ in the SNDPD gives

$$u[k] = x[k] \left(1 - A_{0m} + \sum_{m=0}^{M-1} \sum_{j=1}^{J} a_{jm} \, |x[k - m]|^{j} \right), \tag{A.12}$$

where $1 - A_{0m}$ can be combined to a single parameter $A'_{0M} = 1 - A_{0m}$, which finally yields

$$u[k] = x[k] \left(A'_{0m} + \sum_{m=0}^{M-1} \sum_{j=1}^{J} a_{jm} \, |x[k - m]|^{j} \right), \tag{A.13}$$

The EMP is defined as (2.68):

$$y_{\text{EMP}}[k] = x[k] \cdot \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm} \, |c\,[k - m]|^{j-1}. \tag{A.14}$$

If the EMP is now extended to start from $j = 0$ and use power ^{j} instead of $^{j-1}$ it becomes

$$y_{\text{EMP}}[k] = x[k] \cdot \sum_{j=0}^{J} \sum_{m=0}^{M-1} a_{jm} \, |c\,[k - m]|^{j}, \tag{A.15}$$

where now also the parameter for $j = 0$ can be extracted, yielding

$$y_{\text{EMP}}[k] = x[k] \cdot \left(A_{0m} + \sum_{j=1}^{J} \sum_{m=0}^{M-1} a_{jm} \, |c\,[k - m]|^{j} \right). \tag{A.16}$$

Thus, for polar architectures the SNDPD (A.13) is equivalent to the EMP (A.16).

B State-Space Equations

This appendix section presents all derived state-space equations used in this thesis. Some are already mentioned in the chapters above, but are repeated here to provide the reader a compact overview.

B.1 State-Space Equations of the Polar Capacitive RF-DAC

Here, the state-space equations of the polar RF-DAC are repeated from Section 3.2.1.

B.1.1 Equations without Supply Network

LO=0:

$$c_{on} = C_u \cdot n \tag{B.1a}$$

$$c_{off} = C_u \cdot (N - n) \tag{B.1b}$$

$$r_{on} = \frac{r_{on_p}}{n} \tag{B.1c}$$

$$r_{off} = \frac{r_{on_n}}{N - n} \tag{B.1d}$$

$$\mathbf{K}_{0,n} = \begin{bmatrix} c_n & 0 & 0 \\ 0 & c_{N-n} & 0 \\ 0 & 0 & L \end{bmatrix} \tag{B.1e}$$

$$\mathbf{A}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & 1 - \frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{r_{off}}{r_{on}+r_{off}} & 1 - \frac{r_{off}}{r_{on}+r_{off}} & -\left(R_l + \frac{r_{on}\,r_{off}}{r_{on}+r_{off}}\right) \end{bmatrix} \tag{B.1f}$$

$$\mathbf{B}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} \frac{1}{r_{on}+r_{off}} \\ 1 \\ \frac{r_{off}}{r_{on}+r_{off}} \end{bmatrix} \tag{B.1g}$$

$$\mathbf{E}_{0,n} = \begin{bmatrix} 0 & 0 & R \end{bmatrix} \tag{B.1h}$$

$$\mathbf{F}_{0,n} = 0 \tag{B.1i}$$

B State-Space Equations

LO=1:

$$c_{on} = C_u \cdot n \tag{B.2a}$$

$$c_{off} = C_u \cdot (N - n) \tag{B.2b}$$

$$r_{on} = \frac{r_{on_n}}{n} \tag{B.2c}$$

$$r_{off} = \frac{r_{on_n}}{N - n} \tag{B.2d}$$

$$\mathbf{K}_{1,n} = \begin{bmatrix} c_n & 0 & 0 \\ 0 & c_{N-n} & 0 \\ 0 & 0 & L \end{bmatrix} \tag{B.2e}$$

$$\mathbf{A}_{1,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & 1 - \frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{r_{on}}{r_{on}+r_{off}} \\ -\frac{r_{off}}{r_{on}+r_{off}} & 1 - \frac{r_{off}}{r_{on}+r_{off}} & -\left(R_l + \frac{r_{on}\,r_{off}}{r_{on}+r_{off}} \right) \end{bmatrix} \tag{B.2f}$$

$$\mathbf{B}_{1,n} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{B.2g}$$

$$\mathbf{E}_{1,n} = \begin{bmatrix} 0 & 0 & R \end{bmatrix} \tag{B.2h}$$

$$\mathbf{F}_{1,n} = 0 \tag{B.2i}$$

B.1.2 Equations with Supply Network

LO=0:

$$c_{on} = C_u \cdot n \tag{B.3a}$$

$$c_{off} = C_u \cdot (N - n) \tag{B.3b}$$

$$r_{on} = \frac{r_{on_p}}{n} \tag{B.3c}$$

$$r_{off} = \frac{r_{on_n}}{N - n} \tag{B.3d}$$

$$\mathbf{K}_{0,n} = \begin{bmatrix} L_s & 0 & 0 & 0 & 0 \\ 0 & C_s & 0 & 0 & 0 \\ 0 & 0 & c_n & 0 & 0 \\ 0 & 0 & 0 & c_{N-n} & 0 \\ 0 & 0 & 0 & 0 & L \end{bmatrix} \tag{B.3e}$$

$$\mathbf{A}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -Rs & -1 & 0 & 0 & 0 \\ 1 & -\frac{1}{r_{on}+r_{off}} & \frac{1}{r_{on}+r_{off}} & \frac{1}{r_{on}+r_{off}} & -\frac{r_{off}}{r_{on}+r_{off}} \\ 0 & \frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & \frac{r_{off}}{r_{on}+r_{off}} \\ 0 & \frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{r_{on}}{r_{on}+r_{off}} \\ 0 & \frac{r_{off}}{r_{on}+r_{off}} & -\frac{r_{off}}{r_{on}+r_{off}} & \frac{R_N}{r_{on}+r_{off}} & -\frac{R_l(r_{on}+r_{off})+r_{on}\,r_{off}}{r_{on}+r_{off}} \end{bmatrix} \tag{B.3f}$$

$$\mathbf{B}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{B.3g}$$

$$\mathbf{E}_{0,n} = \begin{bmatrix} 0 & 0 & R_l \end{bmatrix} \tag{B.3h}$$

$$\mathbf{F}_{0,n} = 0 \tag{B.3i}$$

LO=1:

$$c_{on} = C_u \cdot n, \tag{B.4a}$$

$$c_{off} = C_u \cdot (N - n), \tag{B.4b}$$

$$r_{on} = \frac{r_{on_n}}{n} \tag{B.4c}$$

$$r_{off} = \frac{r_{on_n}}{N - n} \tag{B.4d}$$

$$\mathbf{K}_{1,n} = \mathbf{K}_{0,n} \tag{B.4e}$$

$$\mathbf{A}_{0,n} = \mathbf{K}_{0,n}^{-1} \begin{bmatrix} -Rs & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & \frac{r_{off}}{r_{on}+r_{off}} \\ 0 & 0 & -\frac{1}{r_{on}+r_{off}} & -\frac{1}{r_{on}+r_{off}} & -\frac{r_{on}}{r_{on}+r_{off}} \\ 0 & 0 & -\frac{r_{off}}{r_{on}+r_{off}} & \frac{R_N}{r_{on}+r_{off}} & -\frac{R_l(r_{on}+r_{off})+r_{on}\,r_{off}}{r_{on}+r_{off}} \end{bmatrix} \tag{B.4f}$$

$$\mathbf{B}_{0,n} = \mathbf{B}_{1,n} \tag{B.4g}$$

$$\mathbf{E}_{0,n} = \mathbf{E}_{1,n} \tag{B.4h}$$

$$\mathbf{F}_{0,n} = \mathbf{F}_{1,n} \tag{B.4i}$$

B.2 State-Space Equations of the Quadrature Capacitive RF-DAC

The state-space matrices for the quadrature RF-DAC circuits shown in Fig. 3.6 are given below.

$\mathrm{LO_I = 0, LO_Q = 0}$:

$$r_{on_I} = \frac{r_{on_p}}{n_I} \tag{B.5a}$$

$$r_{on_Q} = \frac{r_{on_p}}{n_Q} \tag{B.5b}$$

$$r_{off} = \frac{r_{on_n}}{N - n_I - n_Q} \tag{B.5c}$$

$$C_I = C_u \cdot n_I \tag{B.5d}$$

$$C_Q = C_u \cdot n_Q \tag{B.5e}$$

$$C_{off} = C_u \cdot (N - n_I - n_Q) \tag{B.5f}$$

$$R = \frac{1}{\frac{1}{r_{on_I}} + \frac{1}{r_{on_Q}} + \frac{1}{r_{off}}} \tag{B.5g}$$

$$\mathbf{K}_{0,0,n_I,n_Q} = \begin{bmatrix} C_I \cdot \frac{r_{on_I}}{R} & 0 & 0 & 0 \\ 0 & r_{on_Q} \cdot C_Q & 0 & 0 \\ 0 & 0 & r_{off} \cdot C_{off} & 0 \\ 0 & 0 & 0 & L \end{bmatrix} \tag{B.5h}$$

$$\mathbf{A}_{0,0,n_I,n_Q} = \mathbf{K}_{0,0,n_I,n_Q}^{-1} \cdot \begin{bmatrix} -\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & \frac{1}{r_{on_Q}} & -\frac{1}{r_{off}} & 1 \\ 1 - R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -1 + \frac{R}{r_{on_Q}} & -\frac{R}{r_{off}} & R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & -1 + \frac{R}{r_{off}} & -R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & \frac{R}{r_{off}} & -R_L - R \end{bmatrix} \tag{B.5i}$$

$$\mathbf{B}_{0,0,n_I,n_Q} = \mathbf{K}_{0,0,n_I,n_Q}^{-1} \cdot \begin{bmatrix} \frac{1}{r_{off}} \\ \frac{R}{r_{off}} \\ 1 - \frac{R}{r_{off}} \\ 1 - \frac{R}{r_{off}} \end{bmatrix} \tag{B.5j}$$

$\mathrm{LO_I = 0, LO_Q = 1}$:

$$r_{on_I} = \frac{r_{on_p}}{n_I} \tag{B.6a}$$

$$r_{on_Q} = \frac{r_{on_n}}{n_Q} \tag{B.6b}$$

$$r_{off} = \frac{r_{on_n}}{N - n_I - n_Q} \tag{B.6c}$$

$$C_I = C_u \cdot n_I \tag{B.6d}$$

$$C_Q = C_u \cdot n_Q \tag{B.6e}$$

$$C_{off} = C_u \cdot (N - n_I - n_Q) \tag{B.6f}$$

$$R = \frac{1}{\frac{1}{r_{on_I}} + \frac{1}{r_{on_Q}} + \frac{1}{r_{off}}} \tag{B.6g}$$

$$\mathbf{K}_{0,1,n_I,n_Q} = \begin{bmatrix} C_I \cdot \frac{r_{on_I}}{R} & 0 & 0 & 0 \\ 0 & r_{on_Q} \cdot C_Q & 0 & 0 \\ 0 & 0 & r_{off} \cdot C_{off} & 0 \\ 0 & 0 & 0 & L \end{bmatrix} \tag{B.6h}$$

$$\mathbf{A}_{0,1,n_I,n_Q} = \mathbf{K}_{0,1,n_I,n_Q}^{-1} \cdot \begin{bmatrix} -\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & \frac{1}{r_{on_Q}} & -\frac{1}{r_{off}} & 1 \\ 1 - R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -1 + \frac{R}{r_{on_Q}} & -\frac{R}{r_{off}} & R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & -1 + \frac{R}{r_{off}} & -R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & \frac{R}{r_{off}} & -R_L - R \end{bmatrix} \tag{B.6i}$$

$$\mathbf{B}_{0,1,n_I,n_Q} = \mathbf{K}_{0,1,n_I,n_Q}^{-1} \cdot \begin{bmatrix} \frac{1}{r_{on_Q}} + \frac{1}{r_{off}} \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) \\ 1 - R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) \\ 1 - R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) \end{bmatrix} \tag{B.6j}$$

$\text{LO}_\mathbf{I} = \mathbf{1}, \text{LO}_\mathbf{Q} = \mathbf{0}$:

$$r_{on_I} = \frac{r_{on_n}}{n_I} \tag{B.7a}$$

$$r_{on_Q} = \frac{r_{on_p}}{n_Q} \tag{B.7b}$$

$$r_{on_I} = \frac{r_{on_n}}{N - n_I - n_Q} \tag{B.7c}$$

$$C_I = C_u \cdot n_I \tag{B.7d}$$

$$C_Q = C_u \cdot n_Q \tag{B.7e}$$

$$C_{off} = C_u \cdot (N - n_I - n_Q) \tag{B.7f}$$

$$R = \frac{1}{\frac{1}{r_{on_I}} + \frac{1}{r_{on_Q}} + \frac{1}{r_{off}}} \tag{B.7g}$$

$$\mathbf{K}_{1,0,n_I,n_Q} = \begin{bmatrix} C_I \cdot \frac{r_{on_I}}{R} & 0 & 0 & 0 \\ 0 & r_{on_Q} \cdot C_Q & 0 & 0 \\ 0 & 0 & r_{off} \cdot C_{off} & 0 \\ 0 & 0 & 0 & L \end{bmatrix} \tag{B.7h}$$

$$\mathbf{A}_{1,0,n_I,n_Q} = \mathbf{K}_{1,0,n_I,n_Q}^{-1} \cdot \begin{bmatrix} -1 + \frac{R}{r_{on_I}} & 1 - R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{off}} & R \\ \frac{1}{r_{on_I}} & -\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) & -\frac{1}{r_{off}} & 1 \\ -\frac{R}{r_{on_I}} & -1 + R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) & -1 + \frac{R}{r_{off}} & -R \\ -\frac{R}{r_{on_I}} & -1 + R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) & \frac{R}{r_{off}} & -R_L - R \end{bmatrix} \tag{B.7i}$$

$$\mathbf{B}_{1,0,n_I,n_Q} = \mathbf{K}_{1,0,n_I,n_Q}^{-1} \cdot \begin{bmatrix} -1 + R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) \\ \frac{1}{r_{on_I}} + \frac{1}{r_{off}} \\ 1 - R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) \\ 1 - R\left(\frac{1}{r_{on_I}} + \frac{1}{r_{off}}\right) \end{bmatrix} \tag{B.7j}$$

$\mathrm{LO_I = 1, LO_Q = 1}$:

$$r_{on_I} = \frac{r_{on_n}}{n_I} \tag{B.8a}$$

$$r_{on_Q} = \frac{r_{on_n}}{n_Q} \tag{B.8b}$$

$$r_{on_I} = \frac{r_{on_n}}{N - n_I - n_Q} \tag{B.8c}$$

$$C_I = C_u \cdot n_I \tag{B.8d}$$

$$C_Q = C_u \cdot n_Q \tag{B.8e}$$

$$C_{off} = C_u \cdot (N - n_I - n_Q) \tag{B.8f}$$

$$R = \frac{1}{\frac{1}{r_{on_I}} + \frac{1}{r_{on_Q}} + \frac{1}{r_{off}}} \tag{B.8g}$$

$$\mathbf{K}_{1,1,n_I,n_Q} = \begin{bmatrix} C_I \cdot \frac{r_{on_I}}{R} & 0 & 0 & 0 \\ 0 & r_{on_Q} \cdot C_Q & 0 & 0 \\ 0 & 0 & r_{off} \cdot C_{off} & 0 \\ 0 & 0 & 0 & L \end{bmatrix} \tag{B.8h}$$

$$\mathbf{A}_{1,1,n_I,n_Q} = \mathbf{K}_{1,1,n_I,n_Q}^{-1} \cdot \begin{bmatrix} -\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & \frac{1}{r_{on_Q}} & -\frac{1}{r_{off}} & 1 \\ 1 - R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -1 + \frac{R}{r_{on_Q}} & -\frac{R}{r_{off}} & R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & -1 + \frac{R}{r_{off}} & -R \\ -1 + R\left(\frac{1}{r_{on_Q}} + \frac{1}{r_{off}}\right) & -\frac{R}{r_{on_Q}} & \frac{R}{r_{off}} & -R_L - R \end{bmatrix}$$
$$\tag{B.8i}$$

$$\mathbf{B}_{1,1,n_I,n_Q} = \mathbf{K}_{1,1,n_I,n_Q}^{-1} \cdot \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{B.8j}$$

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