Five Outstanding Innovators Under Age 40 Honored at the 56th Design Automation Conference

Engineers from industry giants to academia recognized for contributions to EDA

LOUISVILLE, COLORADO— May 16, 2019— For 56 years, the future of innovation for the design and automation of electronic systems and circuits has been found at the Design Automation Conference (DAC). This year is no different, DAC and its sponsors are pleased to announce the five winners of the Under-40 Innovators Award, sponsored by Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE). The award recognizes five top young innovators, who have made a significant impact in the field of design and automation of electronics.

The winners will be honored before the keynote address on Monday, June 3rd at 56th DAC being held June 2-6, 2019 at the Las Vegas Convention Center, Las Vegas, NV. The honorees will also participate on a panel to discuss *Quantum Computing, AI and IOT*. The panel discussion will held at DAC on Monday, June 3 at 3:00 p.m., moderated by EE Times Editor, Junko Yoshida in the DAC Pavilion.

Registration for DAC is open now. Deadline to register for the complimentary I LOVE DAC exhibit pass is Friday, May 17th. The I LOVE DAC pass allows free access to the DAC exhibits, award ceremonies, five Keynote sessions, the DAC Pavilion sponsored by Cadence, and the Design on Cloud Pavilion sponsored by Google, with daily presentations along with networking receptions each evening.

The 2019 Under 40 Innovation honorees are:

Yunji Chen, Full professor, Institute of Computing Technology, Chinese Academy of Sciences

Yunji Chen graduated from Special Class for Gifted Young, University of Science and Technology of China in 2002, and got his Ph.D. degree from Institute of Computing Technology (ICT), Chinese Academy of Sciences in 2007, both in computer science. Currently, he is a full professor at ICT. He leads the Intelligent Processor Research Center of

ICT to develop the Cambricon deep learning processors. Yunji Chen has co-written one book and more than 100 papers presented at various engineering conferences. He served as the general co-chair of ASPLOS'17, and as a member of the technical program committee for DAC, ISCA, HPCA, MICRO, and ASPLOS. Chen has been listed in MIT Global TR-35 (2015) for his contribution in deep learning processors and has been reported as "leader" and "pioneer" of deep learning processor by Science magazine.

Huichu Liu, Staff Research Scientist, Intel Corporation

Huichu Liu received the B.S. degree in microelectronics from Peking University, Beijing in 2009 and the Ph.D. degree in electrical engineering from the Pennsylvania State University in 2014. While earning her doctorate, she won an IBM Ph.D. Fellowship Award. Huichu interned at IBM's T. J. Watson Research Center, from May-August 2011, and at GlobalFoundries from June -August 2014, respectively. In 2015, Huichu joined Intel Labs as a research scientist for process-optimized microarchitecture design, where she has made multiple innovations and technology transfers for driving energy efficiency breakthroughs in circuits and CPU architecture with novel devices. She is currently a staff research scientist at the Artificial Intelligence Product Group, Intel Movidius. Her research interests include device-circuit co-design of beyond-CMOS logic technologies and emerging non-volatile memories for energy efficient applications and agile hardware design exploration of advanced architectures for machine learning accelerators. Huichu has contributed to 49 publications and holds nine US patents.

Rasit Onur Topaloglu, Senior Hardware Developer & Program Manager, IBM Corp.

Rasit Onur Topaloglu obtained his B.S. in electrical and electronic engineering from Bogazici University, M.S. in computer science, and Ph.D. in computer engineering from University of California, San Diego. He has worked for companies such as Qualcomm, AMD, GlobalFoundries and is currently with IBM. As a senior hardware developer, he focuses on design for manufacturability and design-technology co-optimization. Additionally, he is a program manager responsible for 7nm technology and Power10 microprocessors. He has over 60 peer-reviewed publications and 30 U.S. patents. He serves on the IBM Internet of Things patent review board. His latest book, "Beyond-CMOS Technologies for Next Generation Computer Design," is out now. He has organized seven DAC workshops in previous years, including one – on machine learning – that had more than 100 registrations. He serves as vice chair and professional activities chair of the IEEE Mid-Hudson chapter and secretary of ACM Poughkeepsie. His latest talks include "Compact Qubits for Quantum Computing" and "ACM Code of Ethics and Implications on Artificial Intelligence."

Robert Wille, Professor, Johannes Kepler University Linz, Austria

Robert Wille, a professor at the Johannes Kepler University Linz, Austria, was appointed at the age of 32 as one of the industry's youngest full professors. From 2002 to 2006, he studied computer science at the University of Bremen. After completing his doctorate in 2009 summa cum laude, he did post-doctoral work at the University of Bremen and, since 2013, has served as senior researcher in the cyber-physical systems department of the German Research Center for Artificial Intelligence (DFKI). He's an expert in developing methods for design automation, which he not only applies to the design of conventional circuits and systems, but also to future technologies (including quantum computing, reversible circuits, microfluidic biochips, etc.) as well as complementary fields such as particle-based simulation. He is an interdisciplinary researcher who frequently crosses the boundaries between computer science, electrical engineering, quantum physics, medicine, or even legal sciences. The methods he's developed have created lasting impacts for companies such as Infineon, IBM, or AMD as well as businesses with markets in domains different from the established EDA companies. He has published more than 200 journal and conference papers, which have been presented at various conferences including DAC, DATE, ICCAD, ASP-DAC, MoDELS and TCAD. His honors include a Google Research Award in 2018 as well as best paper awards at the International Conference on Computer-Aided Design in 2013 and the Forum on

Specification and Design Languages in 2010.

Vijay Raghunathan, Professor of Electrical and Computer Engineering, Purdue University

Vijay Raghunathan is a professor of electrical and computer engineering at Purdue University and the director of the Embedded Systems and IoT Lab, which he founded in 2006. He received his M.S. and Ph.D. degrees in electrical engineering from UCLA and his B. Tech. degree in electrical engineering from IIT Madras, India. At Purdue University, his team investigates the design of new hardware and software architectures for next-generation embedded systems, IoT edge devices, and wearable/implantable electronics, with an emphasis on ultra-low power design, micro-scale energy harvesting, edge analytics, and reliable/secure system design. Vijay also holds an appointment as the Anand Rajaraman and Venky Harinarayan Visiting Chair Professor of Computer Science and Engineering at the Indian Institute of Technology (IIT), Madras.

Vijay has co-written more than 100 journal and conference papers (several of which have won best paper and best design awards) and has presented numerous keynotes, invited talks, and tutorials on the above topics. Several of the technologies and systems developed in his lab have been used in academia and industry. He has chaired multiple premier ACM and IEEE conferences and has served on the organizing and technical program committees of many more. He serves as an associate editor of two leading research journals, the ACM Transactions on Embedded Computing Systems (TECS) and the ACM Transactions on Sensor Networks (TOSN). He also serves as an alternate steering committee member of the Industrial Internet Consortium (IIC), one of the largest international consortia on industrial IoT, fog, and edge computing, which has over 250 member organizations. At Purdue, he serves as the founding director of the Professional MS program in the School of ECE.

For additional information on the award and the Design Automation Conference visit https://dac.com/.

About DAC
The Design Automation Conference (DAC) is recognized as the premier event for the design of electronic circuits and systems, and for electronic design automation (EDA) and silicon solutions. A diverse worldwide community representing more than 1,000 organizations attends each year, represented by system designers and architects, logic and circuit designers, validation engineers, CAD managers, senior managers and executives to researchers and academicians from leading universities. More than 75 technical sessions selected by a committee of electronic design experts offer information on recent developments and trends, management practices and new products, methodologies and technologies. A highlight of DAC is its exhibition and suite area with approximately 170 of the leading and emerging EDA, silicon, intellectual property (IP) and design services providers. The conference is sponsored by the Association for Computing Machinery's Special Interest Group on Design Automation (ACM SIGDA), and the Institute of Electrical and Electronics Engineer's Council on Electronic Design Automation (IEEE CEDA).

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Date to post:

Thursday, May 16, 2019 - 16:45

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Exhibit at DAC

DAC is the premier conference devoted to the design and automation of electronic systems (EDA), embedded systems and software (ESS), and intellectual property (IP).

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DAC 2020 Venue

DAC 2020 will be held in San Francisco, California at Moscone Center West. Get details about travel, hotels, and area attractions in one convenient spot.

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